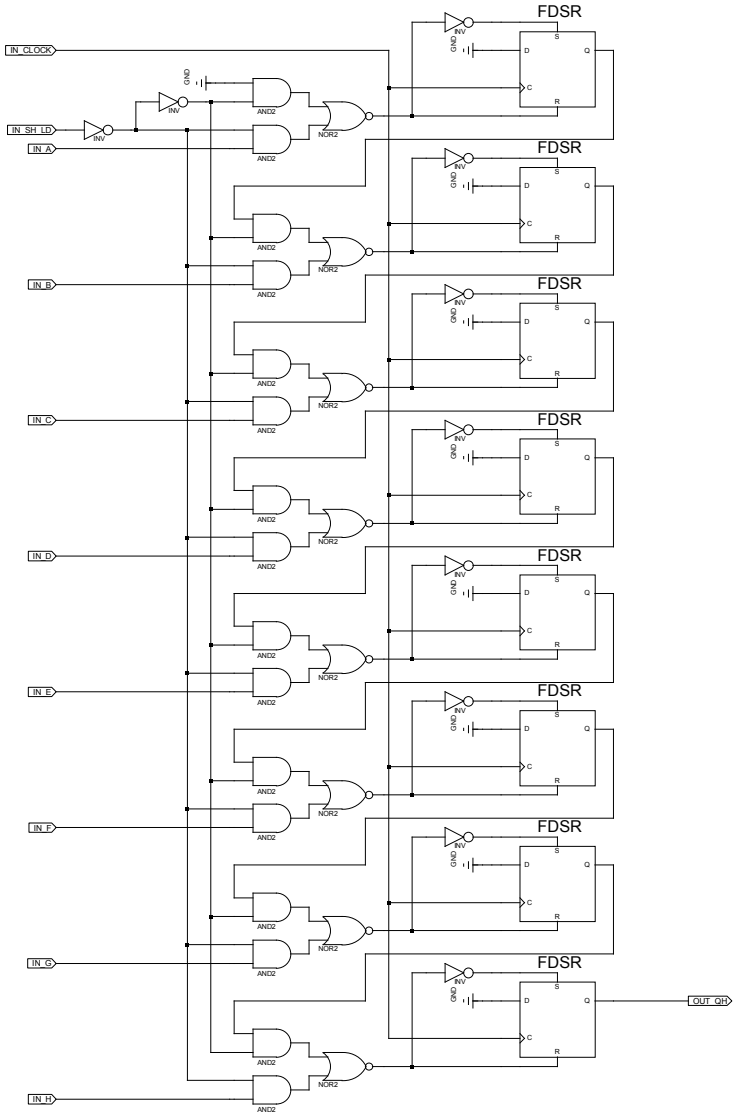
IN_CLOCK
IN_SH_LD
IN_A
IN_B
IN_C
IN_D
IN_E
IN_F
IN_G
IN_H
OUT_QH
INV
GND
AND2
NOR2
FDSR
D
C
S
R
Q

```
--------------------------------------------------------------------------------
-- Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
--------------------------------------------------------------------------------
--   ____  ____
--  /   /\/   /
-- /___/  \  /    Vendor: Xilinx
-- \   \   \/     Version : 14.7
--  \   \         Application : sch2hdl
--  /   /         Filename : hc166.vhf
-- /___/   /\     Timestamp : 04/28/2017 07:44:54
-- \   \  /  \
--  \___\/\___\
--
--Command: sch2hdl -intstyle ise -family xc9500 -flat -suppress -vhdl
D:/Dokumenty/Logic_74HC166/hc166.vhf -w D:/Dokumenty/Logic_74HC166/hc166.sch
--Design Name: hc166
--Device: xc9500
--Purpose:
--    This vhdl netlist is translated from an ECS schematic. It can be
--    synthesized and simulated, but it should not be modified.
--

library ieee;
use ieee.std_logic_1164.ALL;
use ieee.numeric_std.ALL;
library UNISIM;
use UNISIM.Vcomponents.ALL;

entity FD_MXILINX_hc166 is
   generic( INIT : bit :=  '0');
   port ( C : in    std_logic;
          D : in    std_logic;
          Q : out   std_logic);
end FD_MXILINX_hc166;

architecture BEHAVIORAL of FD_MXILINX_hc166 is
   attribute BOX_TYPE   : string ;
   signal XLXN_4 : std_logic;
   component GND
      port ( G : out   std_logic);
   end component;
   attribute BOX_TYPE of GND : component is "BLACK_BOX";

   component FDCP
      generic( INIT : bit :=  '0');
      port ( C   : in    std_logic;
             CLR : in    std_logic;
             D   : in    std_logic;
             PRE : in    std_logic;
             Q   : out   std_logic);
   end component;
   attribute BOX_TYPE of FDCP : component is "BLACK_BOX";

begin
   I_36_43 : GND
      port map (G=>XLXN_4);

```

```
57      U0 : FDCP
58      generic map( INIT => INIT)
59         port map (C=>C,
60                   CLR=>XLXN_4,
61                   D=>D,
62                   PRE=>XLXN_4,
63                   Q=>Q);
64
65   end BEHAVIORAL;
66
67
68
69   library ieee;
70   use ieee.std_logic_1164.ALL;
71   use ieee.numeric_std.ALL;
72   library UNISIM;
73   use UNISIM.Vcomponents.ALL;
74
75   entity FDSR_MXILINX_hc166 is
76      generic( INIT : bit :=  '0');
77      port ( C : in    std_logic;
78             D : in    std_logic;
79             R : in    std_logic;
80             S : in    std_logic;
81             Q : out   std_logic);
82   end FDSR_MXILINX_hc166;
83
84   architecture BEHAVIORAL of FDSR_MXILINX_hc166 is
85      attribute BOX_TYPE   : string ;
86      attribute HU_SET     : string ;
87      signal XLXN_6 : std_logic;
88      signal XLXN_7 : std_logic;
89      component OR2
90         port ( I0 : in    std_logic;
91                I1 : in    std_logic;
92                O  : out   std_logic);
93      end component;
94      attribute BOX_TYPE of OR2 : component is "BLACK_BOX";
95
96      component AND2B1
97         port ( I0 : in    std_logic;
98                I1 : in    std_logic;
99                O  : out   std_logic);
100     end component;
101     attribute BOX_TYPE of AND2B1 : component is "BLACK_BOX";
102
103     component FD_MXILINX_hc166
104        generic( INIT : bit :=  '0');
105        port ( C : in    std_logic;
106               D : in    std_logic;
107               Q : out   std_logic);
108     end component;
109
110     attribute HU_SET of U1 : label is "U1_0";
111  begin
112     I_36_83 : OR2
113        port map (I0=>S,
```

```
114                  I1=>XLXN_6,
115                  O=>XLXN_7);
116
117      I_36_96 : AND2B1
118         port map (I0=>R,
119                  I1=>D,
120                  O=>XLXN_6);
121
122      U1 : FD_MXILINX_hc166
123      generic map( INIT => INIT)
124         port map (C=>C,
125                  D=>XLXN_7,
126                  Q=>Q);
127
128   end BEHAVIORAL;
129
130
131
132   library ieee;
133   use ieee.std_logic_1164.ALL;
134   use ieee.numeric_std.ALL;
135   library UNISIM;
136   use UNISIM.Vcomponents.ALL;
137
138   entity hc166 is
139      port ( IN_A     : in    std_logic;
140             IN_B     : in    std_logic;
141             IN_C     : in    std_logic;
142             IN_CLOCK : in    std_logic;
143             IN_D     : in    std_logic;
144             IN_E     : in    std_logic;
145             IN_F     : in    std_logic;
146             IN_G     : in    std_logic;
147             IN_H     : in    std_logic;
148             IN_SH_LD : in    std_logic;
149             OUT_QH   : out   std_logic);
150   end hc166;
151
152   architecture BEHAVIORAL of hc166 is
153      attribute HU_SET     : string ;
154      attribute BOX_TYPE   : string ;
155      signal XLXN_1   : std_logic;
156      signal XLXN_2   : std_logic;
157      signal XLXN_3   : std_logic;
158      signal XLXN_4   : std_logic;
159      signal XLXN_5   : std_logic;
160      signal XLXN_6   : std_logic;
161      signal XLXN_7   : std_logic;
162      signal XLXN_8   : std_logic;
163      signal XLXN_10  : std_logic;
164      signal XLXN_12  : std_logic;
165      signal XLXN_14  : std_logic;
166      signal XLXN_16  : std_logic;
167      signal XLXN_18  : std_logic;
168      signal XLXN_20  : std_logic;
169      signal XLXN_22  : std_logic;
170      signal XLXN_24  : std_logic;
```

```
171      signal XLXN_25  : std_logic;
172      signal XLXN_26  : std_logic;
173      signal XLXN_27  : std_logic;
174      signal XLXN_73  : std_logic;
175      signal XLXN_74  : std_logic;
176      signal XLXN_75  : std_logic;
177      signal XLXN_76  : std_logic;
178      signal XLXN_77  : std_logic;
179      signal XLXN_86  : std_logic;
180      signal XLXN_87  : std_logic;
181      signal XLXN_88  : std_logic;
182      signal XLXN_89  : std_logic;
183      signal XLXN_90  : std_logic;
184      signal XLXN_91  : std_logic;
185      signal XLXN_92  : std_logic;
186      signal XLXN_93  : std_logic;
187      signal XLXN_94  : std_logic;
188      signal XLXN_95  : std_logic;
189      signal XLXN_96  : std_logic;
190      signal XLXN_97  : std_logic;
191      signal XLXN_98  : std_logic;
192      signal XLXN_99  : std_logic;
193      signal XLXN_100 : std_logic;
194      signal XLXN_101 : std_logic;
195      signal XLXN_102 : std_logic;
196      signal XLXN_103 : std_logic;
197      signal XLXN_104 : std_logic;
198      signal XLXN_105 : std_logic;
199      signal XLXN_106 : std_logic;
200      signal XLXN_107 : std_logic;
201      signal XLXN_108 : std_logic;
202      signal XLXN_110 : std_logic;
203      signal XLXN_125 : std_logic;
204      signal XLXN_127 : std_logic;
205      component FDSR_MXILINX_hc166
206         generic( INIT : bit :=  '0');
207         port ( C : in    std_logic;
208                D : in    std_logic;
209                R : in    std_logic;
210                S : in    std_logic;
211                Q : out   std_logic);
212      end component;
213
214      component INV
215         port ( I : in    std_logic;
216                O : out   std_logic);
217      end component;
218      attribute BOX_TYPE of INV : component is "BLACK_BOX";
219
220      component GND
221         port ( G : out   std_logic);
222      end component;
223      attribute BOX_TYPE of GND : component is "BLACK_BOX";
224
225      component NOR2
226         port ( I0 : in    std_logic;
227                I1 : in    std_logic;
```

```
228               O  : out   std_logic);
229      end component;
230      attribute BOX_TYPE of NOR2 : component is "BLACK_BOX";
231
232      component AND2
233         port ( I0 : in    std_logic;
234                I1 : in    std_logic;
235                O  : out   std_logic);
236      end component;
237      attribute BOX_TYPE of AND2 : component is "BLACK_BOX";
238
239      attribute HU_SET of XLXI_52 : label is "XLXI_52_1";
240      attribute HU_SET of XLXI_53 : label is "XLXI_53_2";
241      attribute HU_SET of XLXI_54 : label is "XLXI_54_3";
242      attribute HU_SET of XLXI_55 : label is "XLXI_55_4";
243      attribute HU_SET of XLXI_56 : label is "XLXI_56_5";
244      attribute HU_SET of XLXI_57 : label is "XLXI_57_6";
245      attribute HU_SET of XLXI_58 : label is "XLXI_58_7";
246      attribute HU_SET of XLXI_59 : label is "XLXI_59_8";
247   begin
248      XLXI_52 : FDSR_MXILINX_hc166
249         port map (C=>IN_CLOCK,
250                   D=>XLXN_25,
251                   R=>XLXN_20,
252                   S=>XLXN_1,
253                   Q=>XLXN_102);
254
255      XLXI_53 : FDSR_MXILINX_hc166
256         port map (C=>IN_CLOCK,
257                   D=>XLXN_26,
258                   R=>XLXN_22,
259                   S=>XLXN_2,
260                   Q=>XLXN_103);
261
262      XLXI_54 : FDSR_MXILINX_hc166
263         port map (C=>IN_CLOCK,
264                   D=>XLXN_27,
265                   R=>XLXN_24,
266                   S=>XLXN_3,
267                   Q=>XLXN_104);
268
269      XLXI_55 : FDSR_MXILINX_hc166
270         port map (C=>IN_CLOCK,
271                   D=>XLXN_73,
272                   R=>XLXN_18,
273                   S=>XLXN_4,
274                   Q=>XLXN_105);
275
276      XLXI_56 : FDSR_MXILINX_hc166
277         port map (C=>IN_CLOCK,
278                   D=>XLXN_74,
279                   R=>XLXN_16,
280                   S=>XLXN_5,
281                   Q=>XLXN_106);
282
283      XLXI_57 : FDSR_MXILINX_hc166
284         port map (C=>IN_CLOCK,
```

```
285                  D=>XLXN_75,
286                  R=>XLXN_14,
287                  S=>XLXN_6,
288                  Q=>XLXN_107);
289
290      XLXI_58 : FDSR_MXILINX_hc166
291         port map (C=>IN_CLOCK,
292                  D=>XLXN_76,
293                  R=>XLXN_12,
294                  S=>XLXN_7,
295                  Q=>XLXN_108);
296
297      XLXI_59 : FDSR_MXILINX_hc166
298         port map (C=>IN_CLOCK,
299                  D=>XLXN_77,
300                  R=>XLXN_10,
301                  S=>XLXN_8,
302                  Q=>OUT_QH);
303
304      XLXI_60 : INV
305         port map (I=>XLXN_20,
306                  O=>XLXN_1);
307
308      XLXI_61 : INV
309         port map (I=>XLXN_22,
310                  O=>XLXN_2);
311
312      XLXI_62 : INV
313         port map (I=>XLXN_24,
314                  O=>XLXN_3);
315
316      XLXI_63 : INV
317         port map (I=>XLXN_18,
318                  O=>XLXN_4);
319
320      XLXI_64 : INV
321         port map (I=>XLXN_16,
322                  O=>XLXN_5);
323
324      XLXI_65 : INV
325         port map (I=>XLXN_14,
326                  O=>XLXN_6);
327
328      XLXI_66 : INV
329         port map (I=>XLXN_12,
330                  O=>XLXN_7);
331
332      XLXI_67 : INV
333         port map (I=>XLXN_10,
334                  O=>XLXN_8);
335
336      XLXI_68 : GND
337         port map (G=>XLXN_25);
338
339      XLXI_69 : GND
340         port map (G=>XLXN_26);
341
```

```
342      XLXI_70 : GND
343         port map (G=>XLXN_27);
344
345      XLXI_71 : GND
346         port map (G=>XLXN_73);
347
348      XLXI_72 : GND
349         port map (G=>XLXN_74);
350
351      XLXI_73 : GND
352         port map (G=>XLXN_75);
353
354      XLXI_74 : GND
355         port map (G=>XLXN_76);
356
357      XLXI_75 : GND
358         port map (G=>XLXN_77);
359
360      XLXI_76 : NOR2
361         port map (I0=>XLXN_99,
362                   I1=>XLXN_98,
363                   O=>XLXN_20);
364
365      XLXI_77 : NOR2
366         port map (I0=>XLXN_101,
367                   I1=>XLXN_100,
368                   O=>XLXN_22);
369
370      XLXI_78 : NOR2
371         port map (I0=>XLXN_96,
372                   I1=>XLXN_97,
373                   O=>XLXN_24);
374
375      XLXI_79 : NOR2
376         port map (I0=>XLXN_94,
377                   I1=>XLXN_95,
378                   O=>XLXN_18);
379
380      XLXI_80 : NOR2
381         port map (I0=>XLXN_92,
382                   I1=>XLXN_93,
383                   O=>XLXN_16);
384
385      XLXI_81 : NOR2
386         port map (I0=>XLXN_90,
387                   I1=>XLXN_91,
388                   O=>XLXN_14);
389
390      XLXI_82 : NOR2
391         port map (I0=>XLXN_87,
392                   I1=>XLXN_86,
393                   O=>XLXN_12);
394
395      XLXI_83 : NOR2
396         port map (I0=>XLXN_89,
397                   I1=>XLXN_88,
398                   O=>XLXN_10);
```

```
399
400      XLXI_84 : AND2
401         port map (I0=>XLXN_110,
402                   I1=>XLXN_125,
403                   O=>XLXN_98);
404
405      XLXI_85 : AND2
406         port map (I0=>IN_A,
407                   I1=>XLXN_127,
408                   O=>XLXN_99);
409
410      XLXI_86 : AND2
411         port map (I0=>XLXN_110,
412                   I1=>XLXN_102,
413                   O=>XLXN_100);
414
415      XLXI_87 : AND2
416         port map (I0=>IN_B,
417                   I1=>XLXN_127,
418                   O=>XLXN_101);
419
420      XLXI_88 : AND2
421         port map (I0=>XLXN_110,
422                   I1=>XLXN_103,
423                   O=>XLXN_97);
424
425      XLXI_89 : AND2
426         port map (I0=>IN_C,
427                   I1=>XLXN_127,
428                   O=>XLXN_96);
429
430      XLXI_90 : AND2
431         port map (I0=>XLXN_110,
432                   I1=>XLXN_104,
433                   O=>XLXN_95);
434
435      XLXI_91 : AND2
436         port map (I0=>IN_D,
437                   I1=>XLXN_127,
438                   O=>XLXN_94);
439
440      XLXI_92 : AND2
441         port map (I0=>XLXN_110,
442                   I1=>XLXN_105,
443                   O=>XLXN_93);
444
445      XLXI_93 : AND2
446         port map (I0=>IN_E,
447                   I1=>XLXN_127,
448                   O=>XLXN_92);
449
450      XLXI_94 : AND2
451         port map (I0=>XLXN_110,
452                   I1=>XLXN_106,
453                   O=>XLXN_91);
454
455      XLXI_95 : AND2
```

```
456         port map (I0=>IN_F,
457                   I1=>XLXN_127,
458                   O=>XLXN_90);
459
460      XLXI_96 : AND2
461         port map (I0=>XLXN_110,
462                   I1=>XLXN_107,
463                   O=>XLXN_86);
464
465      XLXI_97 : AND2
466         port map (I0=>IN_G,
467                   I1=>XLXN_127,
468                   O=>XLXN_87);
469
470      XLXI_98 : AND2
471         port map (I0=>XLXN_110,
472                   I1=>XLXN_108,
473                   O=>XLXN_88);
474
475      XLXI_99 : AND2
476         port map (I0=>IN_H,
477                   I1=>XLXN_127,
478                   O=>XLXN_89);
479
480      XLXI_108 : GND
481         port map (G=>XLXN_125);
482
483      XLXI_109 : INV
484         port map (I=>XLXN_127,
485                   O=>XLXN_110);
486
487      XLXI_110 : INV
488         port map (I=>IN_SH_LD,
489                   O=>XLXN_127);
490
491   end BEHAVIORAL;
492
493
494
```

```
1   -- Vhdl instantiation template created from schematic
    D:\Dokumenty\Logic_74HC166\hc166.sch - Fri Apr 28 07:51:33 2017
2   --
3   -- Notes:
4   -- 1) This instantiation template has been automatically generated using types
5   -- std_logic and std_logic_vector for the ports of the instantiated module.
6   -- 2) To use this template to instantiate this component, cut-and-paste and then edit.
7   --
8
9      COMPONENT hc166
10     PORT( IN_CLOCK :  IN STD_LOGIC;
11           IN_A :  IN STD_LOGIC;
12           IN_B :  IN STD_LOGIC;
13           IN_C :  IN STD_LOGIC;
14           IN_D :  IN STD_LOGIC;
15           IN_E :  IN STD_LOGIC;
16           IN_F :  IN STD_LOGIC;
17           IN_G :  IN STD_LOGIC;
18           IN_H :  IN STD_LOGIC;
19           OUT_QH  :  OUT   STD_LOGIC;
20           IN_SH_LD   :  IN STD_LOGIC);
21     END COMPONENT;
22
23     UUT: hc166 PORT MAP(
24        IN_CLOCK => ,
25        IN_A => ,
26        IN_B => ,
27        IN_C => ,
28        IN_D => ,
29        IN_E => ,
30        IN_F => ,
31        IN_G => ,
32        IN_H => ,
33        OUT_QH => ,
34        IN_SH_LD =>
35     );
36
```