

DTL NAND Gate Pins



Given a Siemens FZH115 DTL chip (diode transistor logic), which is a 4x NAND DTL gate, datasheet available at <https://datasheet4u.com/pdf-down/F/Z/H/FZH101-Siemens.pdf>, on PDF page 4 - explain the function of pins 1 and 15, described as "N" and going into the base of the transistor inside.

Pins **1** and **15** on the Siemens FZH115 are labeled "**N**" in the internal schematic (PDF page 4). They are **additional control inputs that connect directly to the base node of the gate's switching transistor**, bypassing the diode input network. Understanding them requires looking at how **DTL NAND gates** work.

1. Normal DTL NAND gate structure

A classic **DTL NAND gate** has:

1. **Input diodes** (one per input)
2. A **base resistor** feeding the transistor
3. A **switching transistor** that produces the output

Operation:

- If **any input is LOW**, its diode conducts and **clamps the transistor base low** → transistor OFF → output HIGH.
- If **all inputs are HIGH**, the diodes are reverse-biased → base current flows → transistor ON → output LOW.

So the **diode network performs the NAND function** before the transistor stage.

2. What the "N" input does

Pins **1** and **15 (N)** connect **directly to the base of the transistor**, *after* the diode network.

This means:

- They **override the diode logic**.
- A LOW applied to **N** will **pull the base low directly**, turning the transistor **off regardless of the other inputs**.

So electrically they act like a **direct base clamp**.

3. Why Siemens included it

In the FZ100 DTL family, this extra input was used for **logic expansion / wired gating** between ICs.

Typical purposes:

1 Expanding NAND gates

The N pin lets another stage add inputs **without adding more diodes inside the chip**.

Example:

Gate A output → N input of Gate B

This effectively **adds another NAND condition**.

2 Fast inhibit / enable

Because it goes straight to the transistor base:

- It **turns the transistor off quickly**
- It **overrides normal inputs**

So it can be used as:

- **inhibit**
- **enable**
- **inter-stage gating**

3 Fan-in expansion

DTL gates normally have limited diode fan-in.

The **N input provides an extra logic input path** that doesn't load the diode network.

4. Logical interpretation

For a 2-input NAND with N input:

$Y = \text{NOT}(A \cdot B)$ unless $N = \text{LOW}$

If **N = LOW**:

transistor OFF → $Y = \text{HIGH}$

So **N behaves like an additional NAND input but with stronger priority**.

Equivalent logic approximation:

$Y = \text{NOT}(A \cdot B \cdot N)$

...but electrically it is **not diode-combined**; it is **base-injected**.

5. Why there are two N pins

The chip contains **four NAND gates**, and Siemens placed **two N pins so multiple gates can share expansion lines** without extra package pins.

✓ In short:

Pins **1** and **15 ("N")** are **direct base-injection inputs used for logic expansion or inhibit control**. They bypass the diode input network and can **force the transistor off (output HIGH) regardless of the normal inputs**.

If you'd like, I can also show a **simplified internal schematic of the FZH115 gate and exactly where the N input connects**, which makes the behavior much clearer.