Techniques for 92% Efficient LCD Illumination

Waste Not, Want Not . . .

Jim Williams

INTRODUCTION

In August of 1992 LTC published Application Note 49, "Illumination Circuitry for Liquid Crystal Displays." One notable aspect of this event is that it generated more response *than all previous LTC application notes combined*. This level of interest, along with significant performance advances since AN-49's appearance, justifies further discussion of LCD backlighting circuitry.

This publication includes pertinent information from the previous effort in addition to updated sections and a large body of new material. The partial repetition is a small penalty compared to the benefits of text flow, completeness and time efficient communication. The most noteworthy performance advance is achievement of 92% efficiency for the backlight power supply. Additional new benefits include low voltage operation, synchronizing capability, higher output power for color displays, and extended dimming range.

A practical 92% efficient LCD backlight design is a classic study of compromise in a transduced electronic system. Every aspect of the design is interrelated, and the physical embodiment is an integral part of the electrical circuit. The choice and location of the lamp, wires, display housing and other items has a major effect on electrical characteristics. The greatest care in every detail is required to achieve a practical high efficiency LCD backlight. Getting the lamp to light is just the beginning!

Current generation portable computers and instruments utilize back-lit liquid crystal displays (LCDs). These displays have also appeared in applications ranging from medical equipment to automobiles, gas pumps and retail terminals. Cold Cathode Fluorescent Lamps (CCFLs) provide the highest available efficiency for backlighting the display. These lamps require high voltage AC to operate, mandating an efficient high voltage DC-AC converter. In addition to good efficiency, the converter should deliver the lamp drive in the form of a sine wave. This is desirable to minimize RF emissions. Such emissions can cause interference with other devices, as well as degrading overall operating efficiency. The sine wave excitation also provides optimal current-to-light conversion in the lamp. The circuit should also permit lamp intensity control from zero to full brightness with no hysteresis or "pop-on."

The LCD also requires a bias supply for contrast control. The supply's output should be regulated, and variable over a considerable range.

The small size and battery powered operation associated with LCD equipped apparatus mandate low component count and high efficiency for these circuits. Size constraints place severe limitations on circuit architecture and long battery life is usually a priority. Laptop and hand held portable computers offer an excellent example. The CCFL and its power supply are responsible for almost 50% of the battery drain. Additionally, these components, including PC board and all hardware, usually must fit within the LCD enclosure with a height restriction of 0.25".

Cold Cathode Fluorescent Lamps (CCFLs)

Any discussion of CCFL power supplies must consider lamp characteristics. These lamps are complex transducers, with many variables affecting their ability to convert electrical current to light. Factors influencing conversion efficiency include the lamp's current, temperature, drive waveform characteristics, length, width, gas constituents and the proximity to nearby conductors.

These and other factors are interdependent, resulting in a complex overall response. Figures 1 through 4 show some typical characteristics. A review of these curves hints at the difficulty in predicting lamp behavior as operating conditions vary. The lamp's current and temperature are

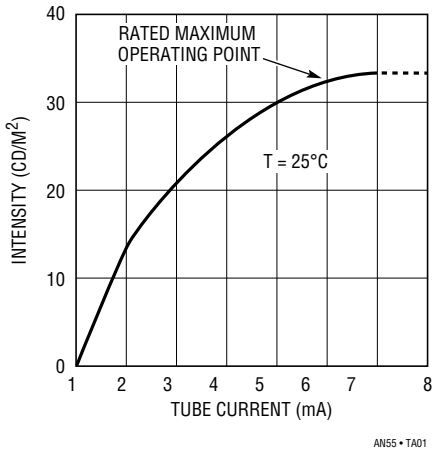


Figure 1. Emissivity for a Typical 6mA Lamp. Curve Flattens Badly Above 6mA

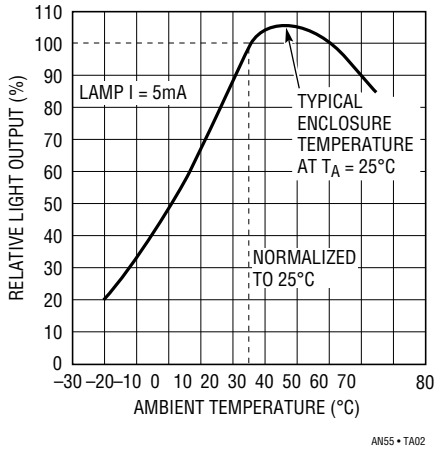


Figure 2. Ambient Temperature Effects on Emissivity of a Typical 5mA Lamp. Lamp and Enclosure Must Come to Thermal Steady State Before Measurements are Made

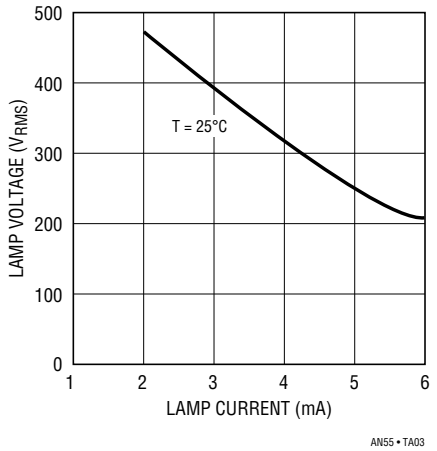


Figure 3. Current vs Voltage for a Lamp in the Operating Region

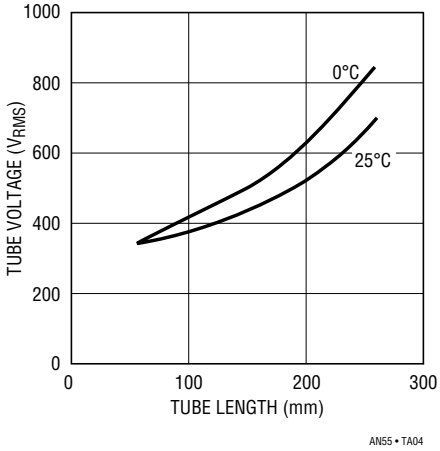
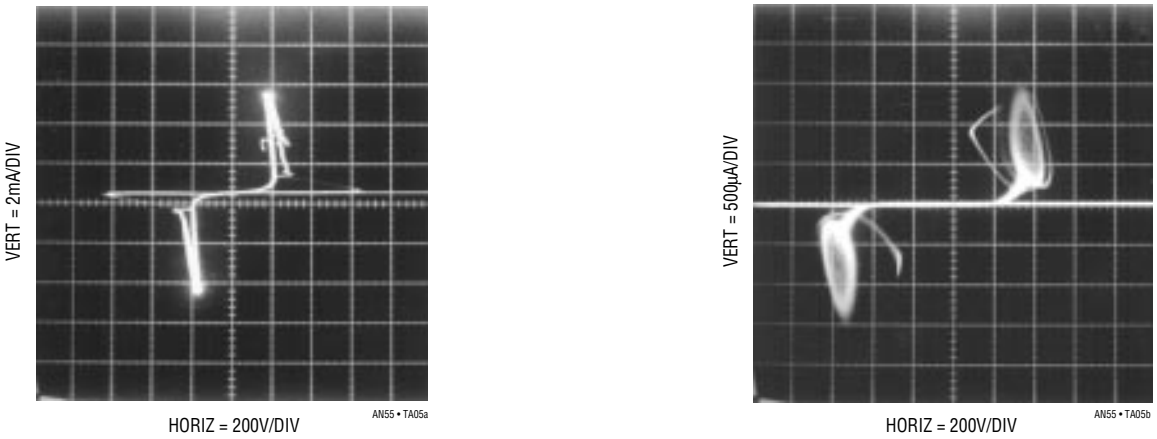


Figure 4. Running Voltage vs Lamp Length at Two Temperatures. Start-Up Voltages are Usually 50% to 200% Higher Over Temperature

clearly critical to emission, although electrical efficiency may not necessarily correspond to the best optical efficiency point. Because of this, both electrical and photometric evaluation of a circuit is often required. It is possible, for example, to construct a CCFL circuit with 94% electrical efficiency which produces less light output than an approach with 80% electrical efficiency (see Appendix J, "A Lot of Cut-Off Ears and No Van Goghs—Some Not-So-Great Ideas." Similarly, the performance of a very well matched lamp-circuit combination can be severely degraded by a lossy display enclosure or excessive high voltage wire lengths. Display enclosures with too much conducting material near the lamp have huge losses due to capacitive coupling. A poorly designed display enclosure can easily degrade efficiency by 20%. High voltage wire runs typically cause 1% loss per inch of wire.

CCFL Load Characteristics

These lamps are a difficult load to drive, particularly for a switching regulator. They have a "negative resistance" characteristic; the starting voltage is significantly higher than the operating voltage. Typically, the start voltage is about 1000V, although higher and lower voltage lamps are common. Operating voltage is usually 300V to 400V, although other lamps may require different potentials. The lamps will operate from DC, but migration effects within the lamp will quickly damage it. As such, the waveform must be AC. No DC content should be present.



5A **5B**

Figure 5. Negative Resistance Characteristic for Two CCFL Lamps. "Snap-Back" is Readily Apparent, Causing Oscillation in 5B. These Characteristics Complicate Power Supply Design

Figure 5A shows an AC driven lamp's characteristics on a curve tracer. The negative resistance induced "snap-back" is apparent. In Figure 5B another lamp, acting against the curve tracer's drive, produces oscillation. These tendencies, combined with the frequency compensation problems associated with switching regulators, can cause severe loop instabilities, particularly on start-up. Once the lamp is in its operating region it assumes a linear load characteristic, easing stability criteria. Lamp operating frequencies are typically 20kHz to 100kHz and a sine-like waveform is preferred. The sine drive's low harmonic content minimizes RF emissions, which could cause interference and efficiency degradation.[1] A further benefit to the continuous sine drive is its low crest factor and controlled rise times, which are easily handled by the CCFL. CCFL's RMS current-to-light output efficiency is degraded by fast rise high crest factor drive waveforms.[2]

CCFL Power Supply Circuits

Figure 6's circuit meets CCFL drive requirements. Efficiency is 88% with an input voltage range of 4.5V to 20V. This efficiency figure can be degraded by about 3% if the LT1172 V_{IN} pin is powered from the same supply as the main circuit V_{IN} terminal. Lamp intensity is continuously and smoothly variable from zero to full intensity. When power is applied the LT1172 switching regulator's feedback pin is below the device's internal 1.2V reference, causing full duty cycle modulation at the V_{SW} pin (Trace A, Figure 7). L2 conducts current (Trace B) which flows from L1's center tap, through the transistors, into L2. L2's current is deposited in switched fashion to ground by the regulator's action.

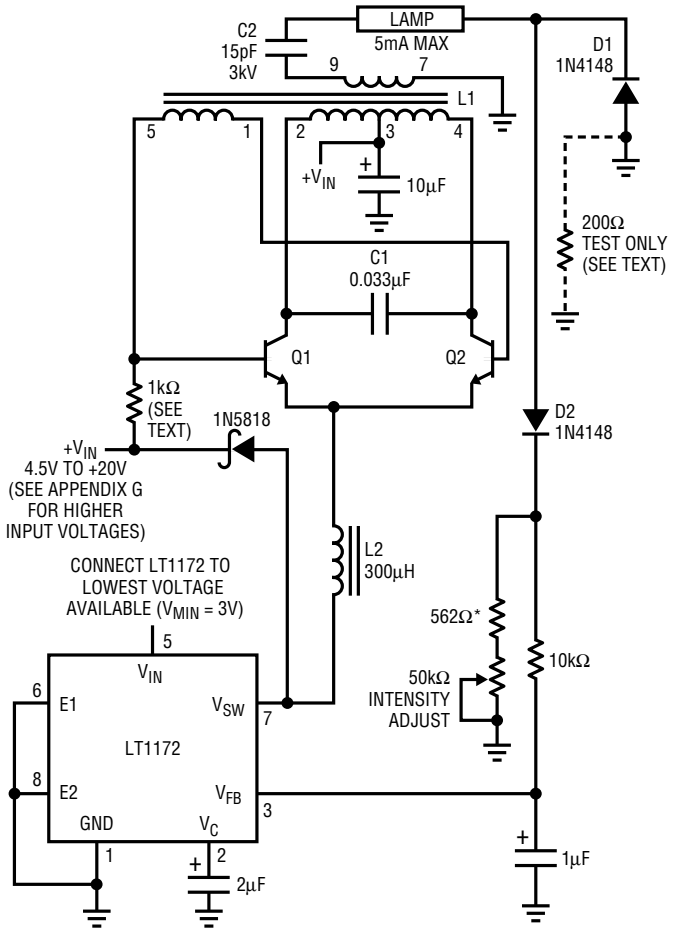
L1 and the transistors comprise a current driven Royer class converter [3] which oscillates at a frequency primarily set by L1's characteristics (including its load) and the 0.033µF capacitor. LT1172 driven L2 sets the magnitude of the Q1-Q2 tail current, hence L1's drive level. The 1N5818 diode maintains L2's current flow when the LT1172 is off. The LT1172's 100kHz clock rate is asynchronous with respect to the push-pull converter's (60kHz) rate, accounting for Trace B's waveform thickening.

The 0.033µF capacitor combines with L1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors (Traces C and D respectively). L1 furnishes voltage step-up, and about $1400V_{P-P}$ appears at its secondary (Trace E). Current flows through the 15pF capacitor into the lamp. On negative waveform cycles the lamp's current is steered to ground via D1. Positive waveform cycles are directed, via D2, to the ground referred 562Ω-50k potentiometer chain. The positive half-sine appearing across the resistors (Trace F) represents 1/2 the lamp

Note 1: Many of the characteristics of CCFLs are shared by so-called "Hot" cathode fluorescent lamps. See Appendix A, "Hot" Cathode Fluorescent Lamps.

Note 2: See Appendix J. "A Lot of Cut-Off Ears and No Van Goghs—Some Not-So-Great Ideas."

Note 3: See Appendix I, "Who Was Royer and What Did He Design?" See also reference 2.

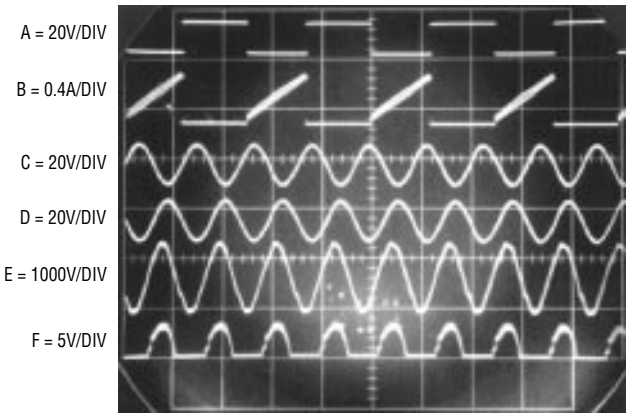


C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 OR MKP-20 (GERMAN) RECOMMENDED
L1 = SUMIDA 6345-020 OR COILTRONICS CTX110092-1
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = COILTRONICS CTX300-4
Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001
*= 1% FILM RESISTOR
DO NOT SUBSTITUTE COMPONENTS

COILTRONICS (305) 781-8900, SUMIDA (708) 956-0666

Figure 6. An 88% Efficiency Cold Cathode Fluorescent Lamp (CCFL) Power Supply

current. This signal is filtered by the 10k-1µF pair and presented to the LT1172's feedback pin. This connection closes a control loop which regulates lamp current. The 2µF capacitor at the LT1172's V_C pin provides stable loop compensation. The loop forces the LT1172 to switch-mode modulate L2's average current to whatever value is required to maintain a constant current in the lamp. The constant current's value, and hence lamp intensity, may be varied with the potentiometer. The constant current drive allows full 0%-100% intensity control with no lamp dead zones or "pop-on" at low intensities.[4] Additionally, lamp



A AND B HORIZ = 4µs/DIV
C THRU F HORIZ = 20µs/DIV
TRIGGERS FULLY INDEPENDENT

Figure 7. Waveforms for the Cold Cathode Fluorescent Lamp Power Supply. Note Independent Triggering on Traces A and B, and C through F

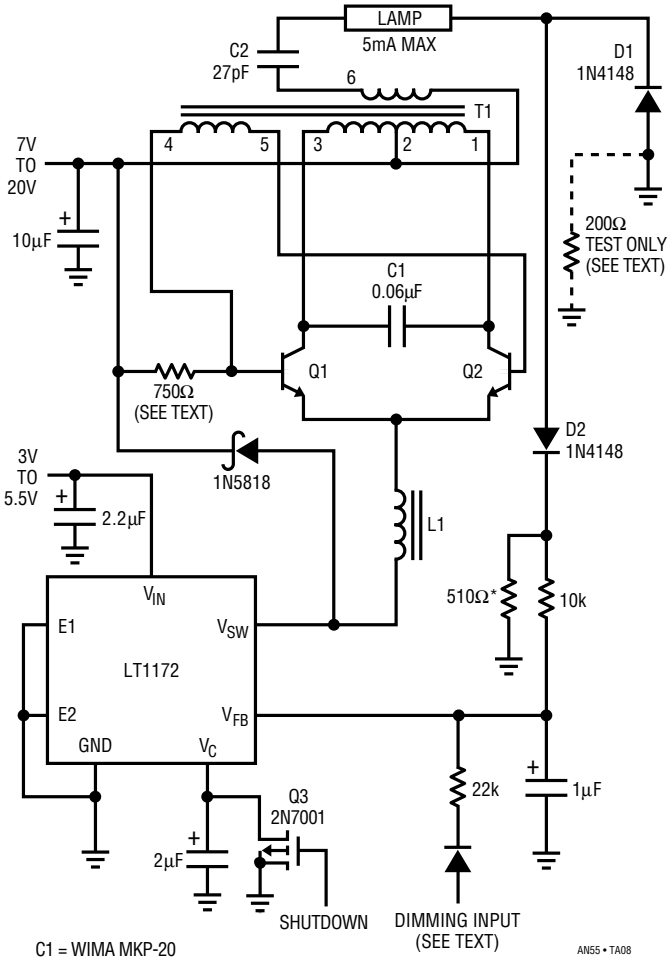
life is enhanced because current cannot increase as the lamp ages.

This circuit's 0.1% line regulation is notably better than some other approaches. This tight regulation prevents lamp intensity variation when abrupt line changes occur. This typically happens when battery powered apparatus is connected to an AC powered charger. The circuit's excellent line regulation derives from the fact that L1's drive waveform never changes shape as input voltage varies. This characteristic permits the simple 10kΩ-1µF RC to produce a consistent response. The RC averaging characteristic has serious error compared to a true RMS conversion, but the error is constant and "disappears" in the 562Ω shunt's value.

This circuit is similar to one previously described[5] but its 88% efficiency is 6% higher. The efficiency improvement is primarily due to the transistor's higher gain and lower saturation voltage. The base drive resistor's value (nominally 1kΩ) should be selected to provide full V_{CE} saturation without inducing base overdrive or beta starvation. A procedure for doing this is described in the following section, "General Measurement and Optimization Considerations."

Note 4: Controlling a nonlinear load's current, instead of its voltage, permits applying this circuit technique to a wide variety of nominally evil loads. See Appendix H, "Related Circuits."

Note 5: See "Illumination Circuitry for Liquid Crystal Displays," Linear Technology Corporation, Application Note 49, August 1992.



C1 = WIMA MKP-20
L1 = COILTRONICS CTX150-4
Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001
T1 = COILTRONICS CTX110600-1 OR SUMIDA EPS-207
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
* = 1% FILM RESISTOR
DO NOT SUBSTITUTE COMPONENTS

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Figure 8. A 91% Efficient CCFL Supply for 5mA Loads Features Shutdown and Dimming Inputs

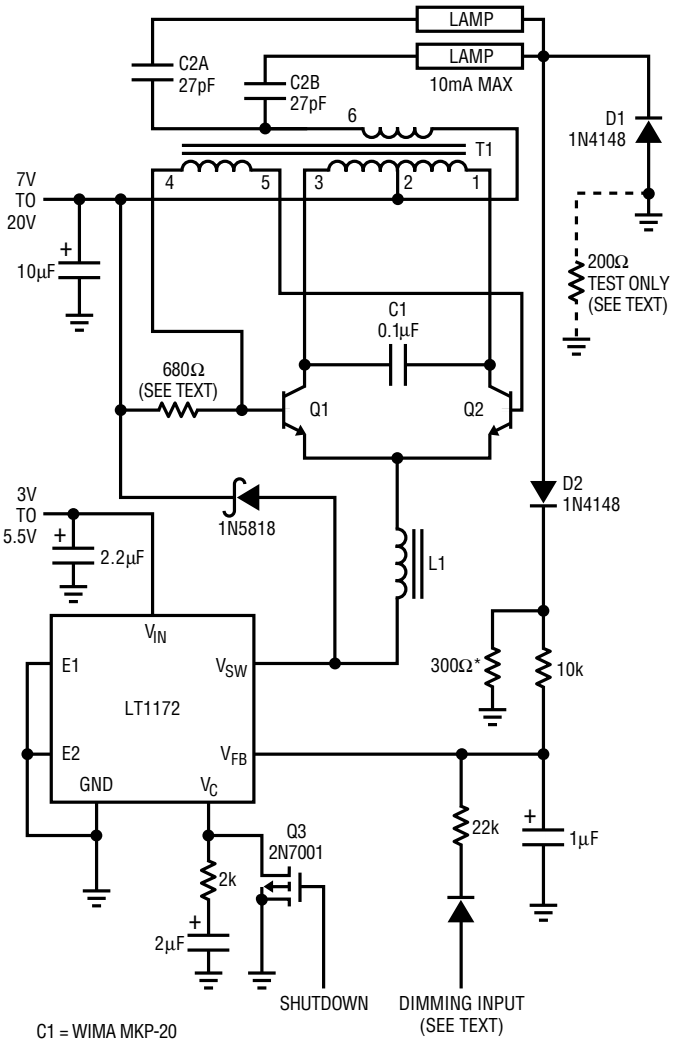

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Figure 9. A 92% Efficient CCFL Supply for 10mA Loads Features Shutdown and Dimming Inputs. Two Lamps are Typical of Color Displays

Figure 8's circuit is similar, but uses a transformer with lower copper and core losses to increase efficiency to 91%. The trade-off is slightly larger transformer size. Value shifts in C1, L2 and the base drive resistor reflect different transformer characteristics. This circuit also features shutdown via Q3 and a DC or pulse width controlled dimming input. Appendix F, "Intensity Control and Shutdown Methods," details operation of these features. Figure 9, directly derived from Figure 8, produces 10mA output to drive color LCD's at 92% efficiency. The slight efficiency improvement comes from a reduction in LT1172 "housekeeping" current as a percentage of total current drain. Value changes in components are the result of higher power operation. The most significant change involves driving two lamps. Accommodating two lamps involves separate ballast capacitors but circuit operation is similar. Two lamp designs reflect slightly different loading back through the transformer's primary. C2 usually ends up in the 10pF to 47pF range. Note that C2A and B appear with their lamp loads in parallel across the transformer's secondary. As such, C2's value is often smaller than in a single lamp circuit using the same type lamp. Ideally the

transformer's secondary current splits evenly between the C2-lamp branches, with the total load current being regulated. In practice, differences between C2A and B and differences in lamps and lamp wiring layout preclude a perfect current split. Practically, these differences are small, and the lamps appear to emit equal amounts of light. Layout and lamp matching can influence C2's value. Some techniques for dealing with these issues appear in the text section, "Layout Issues."

General Measurement and Optimization Considerations

Several points should be kept in mind when observing operation of these circuits. L1's high voltage secondary can only be monitored with a wideband, high voltage probe fully specified for this type of measurement. *The vast majority of oscilloscope probes will break down and fail if used for this measurement.*[6] Tektronix probe types P-6007 and P-6009 (acceptable in some cases) or types P6013A and P6015 (preferred) probes must be used to read L1's output.

Another consideration involves observing waveforms. The LT1172's switching frequency is completely asynchronous from the Q1-Q2 Royer converter's switching. As such, most oscilloscopes cannot simultaneously trigger and display all the circuit's waveforms. Figure 7 was obtained using a dual beam oscilloscope (Tektronix 556). LT1172 related Traces A and B are triggered on one beam, while the remaining traces are triggered on the other beam. Single beam instruments with alternate sweep and trigger switching (e.g., Tektronix 547) can also be used, but are less versatile and restricted to four traces.

Obtaining and verifying high efficiency[7] requires some amount of diligence. The optimum efficiency values given for C1 and C2 are typical, and will vary for specific types of lamps. An important realization is that the term "lamp" includes the *total* load seen by the transformer's secondary. This load, reflected back to the primary, sets transformer input impedance. The transformer's input impedance forms an integral part of the LC tank that produces the high voltage drive. Because of this, circuit efficiency must be optimized with the wiring, display housing and physical layout arranged *exactly* the same way they will be built in production. Deviations from this procedure will result in lower efficiency than might otherwise be possible. In practice, a "first cut" efficiency optimization with "best guess" lead lengths and the intended lamp in its display housing usually produces results within 5% of the achievable figure. Final values for C1 and C2 may be established when the physical layout to be used in production has been decided on. C1 sets the circuit's resonance point, which varies to some extent with the lamp's characteristic. C2 ballasts the lamp, effectively buffering its negative resistance characteristic. Small values of C2 provide the most load isolation, but require relatively large transformer output voltage for loop closure. Large C2 values minimize transformer output voltage, but degrade load buffering. Also, C1's "best" value is somewhat dependent on the lamp type used. Both C1 and C2 must be selected for given lamp types. Some interaction occurs, but generalized guidelines are possible. Typical values for C1 are 0.01μF to 0.15μF. C2 usually ends up in the 10pF to 47pF range. C1 *must* be a low loss capacitor and substitution of the recommended devices is not recommended. A poor quality dielectric for C1 can easily degrade efficiency by 10%. Before capacitor selection the Q1-Q2 base drive resistor should be set to a value which insures saturation, e.g., 470Ω. Next, C1 and C2 are selected by trying different values for each and iterating towards best efficiency. During this procedure insure that loop closure is maintained by monitoring the LT1172's feedback pin, which should be at 1.23V. Several trials usually produce the optimum C1 and C2 values. Note that the highest efficiencies are not necessarily associated with the most esthetically pleasing waveshapes, particularly at Q1, Q2 and the output. Finally, the base drive resistor's value should be optimized.

Note 6: Don't say we didn't warn you!

Note 7: The term "efficiency" as used here applies to electrical efficiency. In fact, the ultimate concern centers around the efficient conversion of power supply energy into light. Unfortunately, lamp types show considerable deviation in their current-to-light conversion efficiency. Similarly, the emitted light for a given current varies over the life and history of any particular lamp. As such, this publication treats "efficiency" on an electrical basis; the ratio of power removed from the primary supply to the power delivered to the lamp. When a lamp has been selected the ratio of primary supply power to lamp emitted light energy may be measured with the aid of a photometer. This is covered in Appendix D, "Photometric Measurement." See also Appendix K, "Perspectives on Efficiency."

The base drive resistor's value (nominally 1kΩ) should be selected to provide full V_{CE} saturation without inducing base overdrive or beta starvation. This point may be established for any lamp type by determining the peak collector current at full lamp power.

The base resistor should be set at the largest value that ensures saturation for worst case transistor beta. This condition may be verified by varying the base drive resistor about the ideal value and noting small variations in input supply current. The minimum obtainable current corresponds to the best beta vs saturation trade-off. In practice, supply current rises slightly on either side of this point. This "double value" behavior is due to efficiency degradation being caused by either excessive base drive or saturation losses.

Other issues influencing efficiency include lamp wire length and energy leakage from the lamp. The high voltage side of the lamp should have the smallest practical lead length. Excessive length results in radiative losses which can easily reach 3% for a 3 inch wire. Similarly, no metal should contact or be in close proximity to the lamp. This prevents energy leakage which can exceed 10%.[8]

It is worth noting that a custom designed lamp affords the best possible results. A jointly tailored lamp-circuit combination permits precise optimization of circuit operation, yielding highest efficiency.

These considerations should be made with knowledge of other LCD issues. See Appendix B, "Mechanical Design Considerations for Liquid Crystal Displays." This section was guest written by Charles L. Guthrie of Sharp Electronics Corporation.

Special attention should be given to the layout of the circuit board since high voltage is generated at the output. The output coupling capacitor must be carefully located to minimize leakage paths on the circuit board. A slot in the board will further minimize leakage. Such leakage can permit current flow outside the feedback loop, wasting power. In the worst case, long term contamination build-up can increase leakage inside the loop, resulting in starved lamp drive or destructive arcing. It is good practice for minimization of leakage to break the silk screen line which outlines transformer T1. This prevents leakage from the high voltage secondary to the primary. Another technique for minimizing leakage is to evaluate and specify the silk screen ink for its ability to withstand high voltages.

Efficiency Measurement

Once these procedures have been followed efficiency can be measured. Efficiency may be measured by determining lamp current and voltage. Measuring current involves measuring RMS voltage across a temporarily inserted 200Ω, 0.1% resistor in the ground lead of the negative current steering diode. The lamp current is: $I_{LAMP} = E_{RMS}/200\Omega \times 2$. The $\times 2$ factor is necessitated because the diode steering dumps the current to ground on negative cycles. The 200Ω value allows the RMS meter to read with a scale factor numerically identical to the total current. Once this measurement is complete the 200Ω resistor may be deleted and the negative current steering diode again returned directly to ground. Lamp RMS voltage is measured at the lamp with a properly compensated high voltage probe. Multiplying these two results gives power in watts, which may be compared to the DC input supply(s) $E \times I$ product(s). In practice, the lamp's current and voltage contain small out of phase components but their error contribution is negligible.

Both the current and voltage measurements require a wideband True RMS voltmeter. The meter must employ a thermal type RMS converter—the more common logarithmic computing type based instruments are inappropriate because their bandwidth is too low.

The previously recommended high voltage probes are designed to see a 1MΩ-10pF-22pF oscilloscope input. The RMS voltmeters have a 10MΩ input. This difference necessitates an impedance matching network between the probe and the voltmeter. Details on this and other efficiency measurement issues appear in Appendix C, "Achieving Meaningful Efficiency Measurements."

Note 8: A very simple experiment quite nicely demonstrates the effects of energy leakage. Grasping the lamp at its low voltage end (low field intensity) with thumb and forefinger produces almost no change in circuit input current. Sliding the thumb-forefinger combination towards the high voltage (higher field intensity) lamp end produces progressively greater input currents. Don't touch the high voltage lead or you may receive an electrical shock. Repeat: Do not touch the high voltage lead or you may receive an electrical shock.

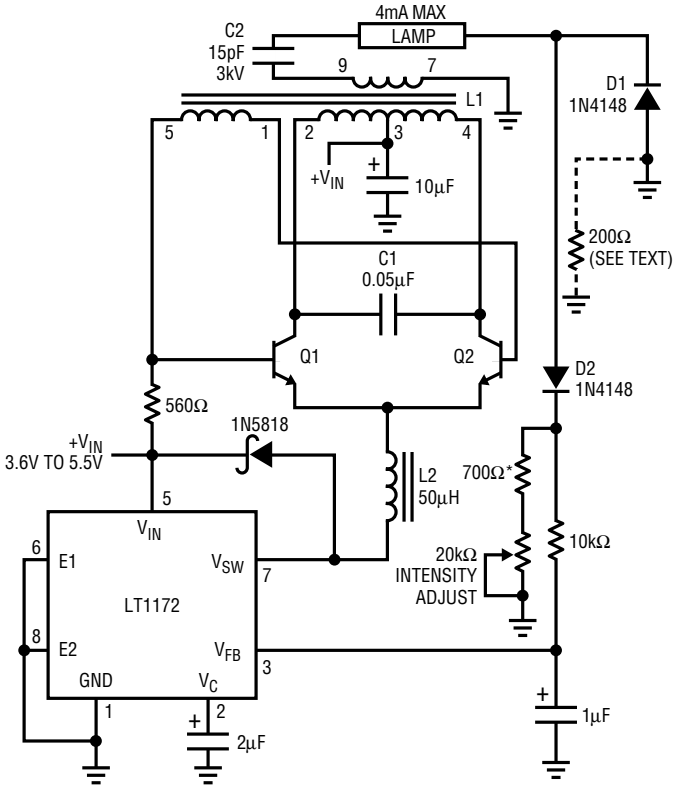

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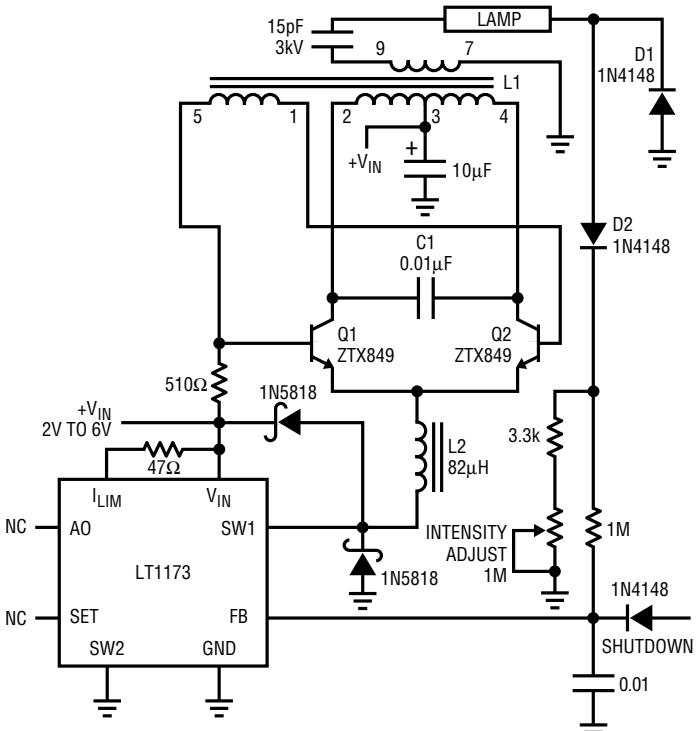
Figure 10. A 4mA Design Intended for Low Voltage Operation. L1's Modified Turns Ratio Allows Operation Down to 3.6V



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L1 = SUMIDA 6345-020 OR COILTRONICS CTX110092-1
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = TOKO 262LYF-0091K
(408) 432-8251
DO NOT SUBSTITUTE COMPONENTS

Figure 11. Low Power CCFL Power Supply. Circuit Controls Lamp Current Over a 1µA to 1mA Range

Low Power CCFL Supplies

Many applications require relatively low power CCFL backlighting. Figure 10's variation, optimized for low voltage inputs, produces 4mA output. Circuit operation is similar to the previous examples. The fundamental difference is L1's higher turns ratio, which accommodates the reduced available drive voltage. The circuit values given are typical, although some variation occurs with various lamps and layouts.

Figure 11's design, the so-called "dim backlight," is optimized for single lamp operation at very low currents. The circuit is meant for use at low input voltages, typically 2V to 6V with a 1mA maximum lamp current. This circuit maintains control down to lamp currents of 1µA, a very dim light! It is intended for applications where the longest possible battery life is desired. Primary supply drain ranges from hundreds of microamperes to 100mA with lamp currents of microamps to 1mA. In shutdown the circuit pulls only 100µA. Maintaining high efficiency at low lamp currents requires modifying the basic design.

Achieving high efficiency at low operating current requires lowering quiescent power drain. To do this the LT1172, a pulse width modulator based device, is replaced with an LT1173. The LT1173 is a Burst Mode™ operation regulator. When this device's feedback pin is too low it delivers a burst of output current pulses, putting energy into the transformer and restoring the feedback point. The regulator maintains control by appropriately modulating the burst duty cycle. The ground referred diode at the V_{SW} pin prevents substrate turn-on due to excessive L2 ring-off.

Burst Mode is a trademark of Linear Technology Corporation.

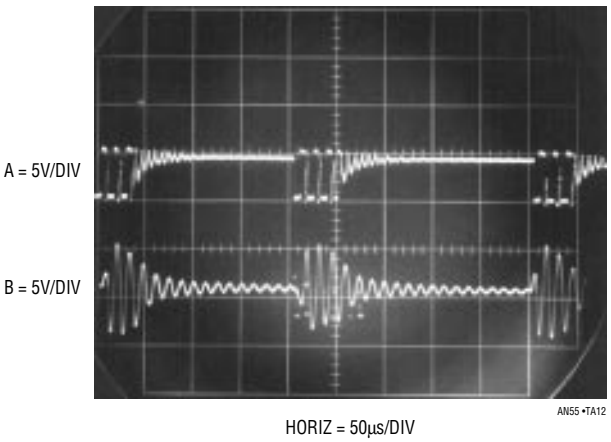

Figure 12. Waveforms for the Low Power CCFL Power Supply. LT1173 Burst Type Regulator (Trace A) Periodically Excites the Resonant High Voltage Converter (Q1 Collector is Trace B)

During the off periods the regulator is essentially shut down. This type of operation limits available output power, but cuts quiescent current losses. In contrast, the other circuit's LT1172 pulse width modulator type regulator maintains "housekeeping" current between cycles. This results in more available output power but higher quiescent currents.

Figure 12 shows operating waveforms. When the regulator comes on (Trace A, Figure 12) it delivers bursts of output current to the L1-Q1-Q2 high voltage converter. The converter responds with bursts of ringing at its resonant frequency.[9] The circuit's loop operation is similar to the previous designs except that L1's drive waveform varies with supply. Because of this, line regulation suffers and the circuit is not recommended for wide ranging inputs.

Some lamps may display non-uniform light emission at very low excitation currents. See the text section, "Extending Illumination Range."

Note 9: The discontinuous energy delivery to the loop causes substantial jitter in the burst repetition rate, although the high voltage section maintains resonance. Unfortunately, circuit operation is in the "chop" mode region of most oscilloscopes, precluding a detailed display. "Alternate" mode operation causes waveform phasing errors, producing an inaccurate display. As such, waveform observation requires special techniques. Figure 12 was taken with a dual beam instrument (Tektronix 556) with both beams slaved to one time base. Single sweep triggering eliminated jitter artifacts. Most oscilloscopes, whether analog or digital, will have trouble reproducing this display.

LCD Bias Supplies

LCDs also require a bias supply for contrast control. The supply's variable output permits adjustment of display contrast. Relatively little power is involved, easing RF radiation and efficiency requirements. The logic sections of display drivers operate from single 5V supplies, but the actual driver outputs swing between +5V and a negative bias potential. Varying this bias causes the display contrast to vary.

An LCD bias generator, developed by Steve Pietkiewicz of LTC, is shown in Figure 13. In this circuit U1 is an LT1173 micropower DC to DC converter. The 3V input is converted to +24V by U1's switch, L2, D1, and C1. The switch pin (SW1) also drives a charge pump composed of C2, C3, D2, and D3 to generate –24V. Line regulation is less than 0.2% from 3.3V to 2V inputs. Load regulation, although suffering somewhat since the –24V output is not directly regulated, measures 2% from a 1mA to 7mA load. The circuit will deliver 7mA from a 2V input at 75% efficiency.

If greater output power is required, Figure 13's circuit can be driven from a +5V source. R1 should be changed to 47Ω and C3 to 47μF. With a 5V input, 40mA is available at 75% efficiency. Shutdown is accomplished by bringing D4's anode to a logic high, forcing the feedback pin of U1 to go above the internal 1.25V reference voltage.

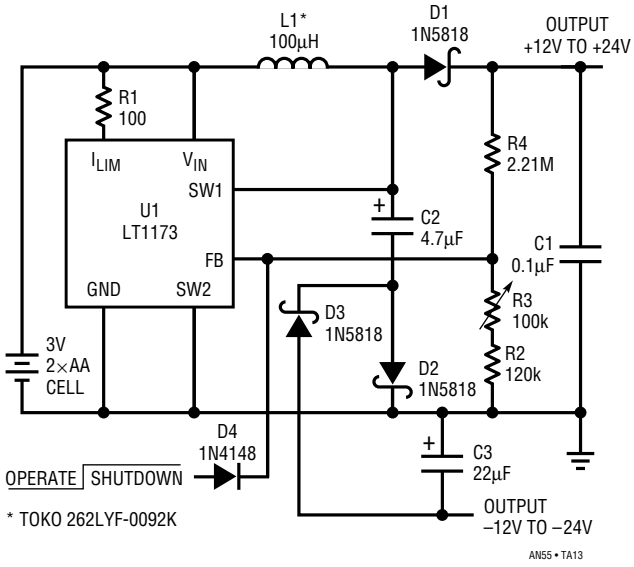

Figure 13. DC to DC Converter Generates LCD Bias

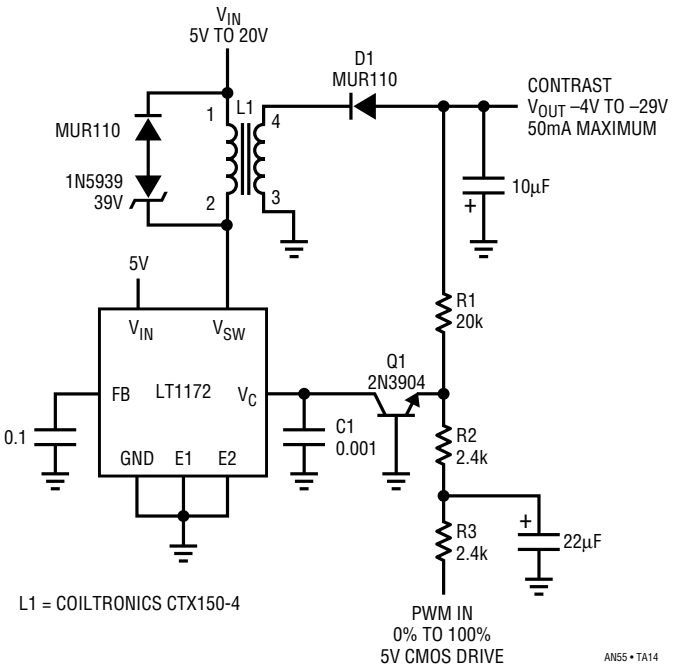

Figure 14. A Transformer Based LCD Contrast Supply. Q1 Level Shifts the Feedback Signal and Functions as a Reference Amplifier

Shutdown current is 110µA from the input source and 36µA from the shutdown signal.

Figure 14 is a transformer based approach to generating LCD bias. The LT1172 drives L1, producing negative flyback events at pin 4. D1 rectifies these events, producing a negative DC output. The R1-R2-R3 string sets feedback at Q1's emitter. Q1, acting as a reference amplifier, biases the LT1172, closing a control loop. C1 provides frequency compensation, stabilizing the loop. In this case, a pulse width modulated signal biases the feedback string, setting operating point and contrast. A 0V to 5V DC signal could also be used. The use of Q1's V_{BE} as a reference introduces a –0.3%/°C temperature coefficient, but this is not deleterious to system operation. Maximum output current is 50mA and efficiency measures about 82%.

Dual Output LCD Bias Voltage Generator

The many different kinds of LCD displays available make programming LCD bias voltage at the time of manufacture attractive. Figure 15's circuit, developed by Jon Dutra of

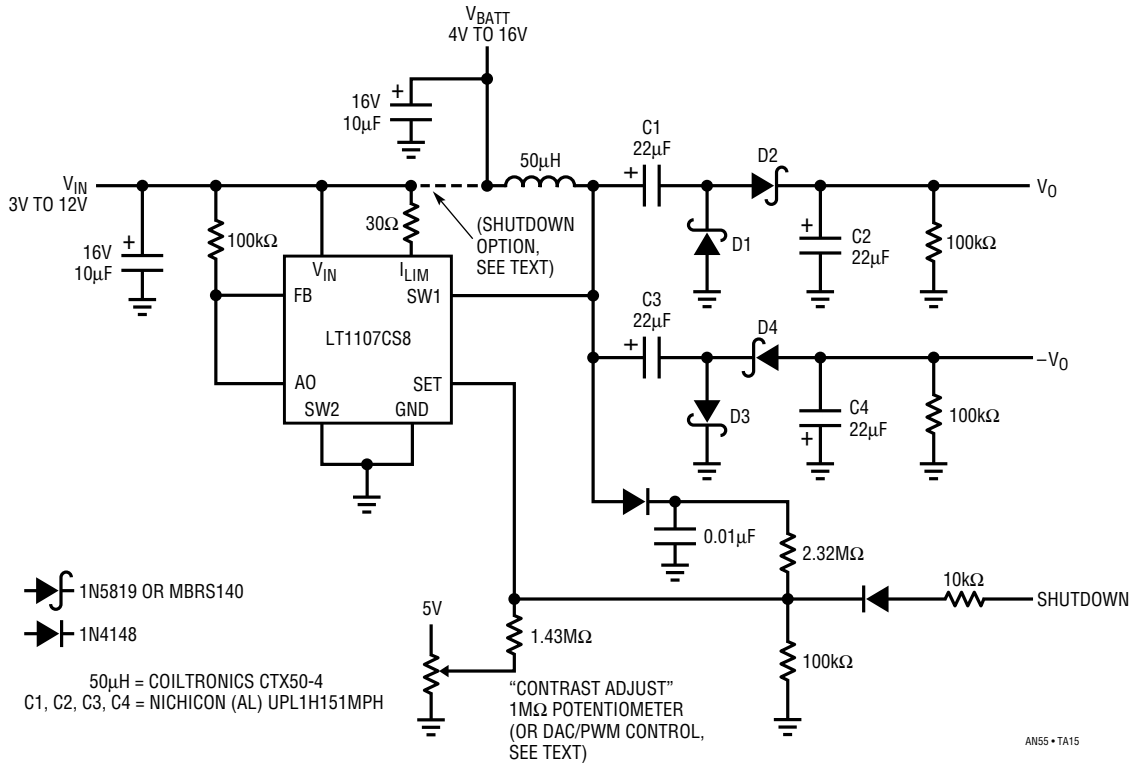

Figure 15. Dual Output LCD Bias Voltage Generator

LTC, is an AC coupled boost topology. The feedback signal is derived separately from the outputs, so loading does not affect loop compensation, although load regulation is somewhat compromised. With 28V out, from 10% to 100% load (4mA to 40mA), the output voltage sags about 0.65V. From 1mA to 40mA load the output voltage drops about 1.4V. This is acceptable for most displays.

Output noise is reduced by using the auxiliary gain block within the LT1107 (see LT1107 data sheet) in the feedback path. This added gain effectively reduces comparator hysteresis and tends to randomize output noise. Output noise is below 30mV over the output load range. Output power increases with V_{BATT}, from about 1.4W with 5V in to about 2W with 8V or more. Efficiency is 80% over a broad output power range. If only a positive or negative output voltage is required, the diodes and capacitors associated with the unused output can be eliminated. The 100kΩ resistor is required on each output to load a parasitic voltage doubler created by D2-D4 shunt capacitance. Without this minimum load, the output voltage can rise to unacceptable levels.

The voltage at the switch pin (SW1) swings from 0V to V_{OUT} plus 2 diode drops. This voltage is AC coupled to the positive output through C1 and D1, and to the negative output through C3 and D3. C1 and C3 have the full RMS output current flowing through them. Most tantalum capacitors are not rated for current flow. Use of a rated tantalum or electrolytic is recommended for reliability. At lower output currents monolithic ceramics are also an option.

The circuit may be shut down in several ways. The easiest is to pull the set pin above 1.25V. This approach consumes 200μA in shutdown. A lower power method is to turn off V_{IN} to the LT1107 by a high side switch or simply disable the input supply (see option in schematic). This drops quiescent current from the V_{BATT} input below 10μA. In both cases V_{OUT} drops to zero volts. In the event $+V_{OUT}$ does not need to drop to zero, C1 and D1 can be eliminated. The output voltage can be adjusted from any voltage above V_{BATT} to 46V. Output voltage can be controlled by the user with DAC, PWM or potentiometer control. Summing currents into the feedback node allows downward adjustment of output voltage.

Layout

The physical layout of the lamp, its leads, the display housing and other high voltage components is an integral part of the circuit. Poor layout can easily degrade efficiency by 25%, and higher layout induced losses have been observed. Producing an optimal layout requires attention to how losses occur. Figure 16 begins our study by examining potential parasitic paths between the transformer's output and the lamp. Parasitic capacitance to AC ground from any point between the transformer output and the lamp creates a path for undesired current flow. Similarly, stray coupling from any point along the lamp's length to AC ground induces parasitic current flow. All parasitic current flow is wasted, causing the circuit to produce more energy to maintain the desired current flow

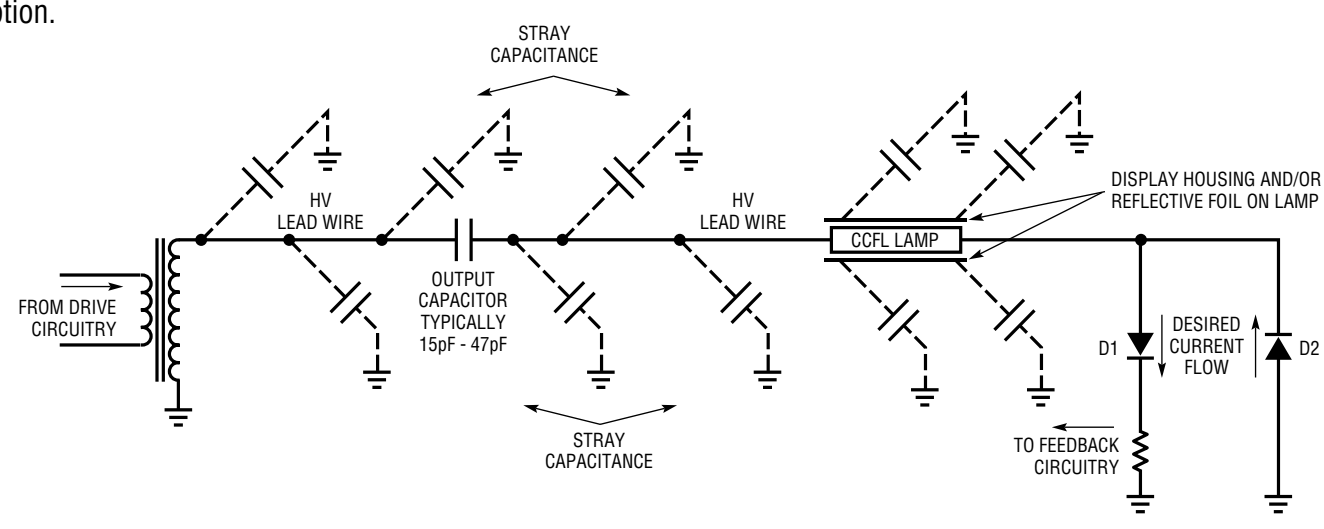

Figure 16. Loss Paths Due to Stray Capacitance in a Practical LCD Installation. Minimizing these Paths is Essential for Good Efficiency

in D1 and D2. The high voltage path from the transformer to the display housing should be as short as possible to minimize losses. A good rule of thumb is to assume 1% efficiency loss per inch of high voltage lead. Any PC board ground or power planes should be relieved by at least 1/4" in the high voltage area. This not only prevents losses, but eliminates arcing paths.

Parasitic losses associated with lamp placement within the display housing require attention. High voltage wire length within the housing must be minimized, particularly for displays using metal construction. Insure that the high voltage is applied to the shortest wire(s) in the display. This may require disassembling the display to verify wire length and layout. Another loss source is the reflective foil commonly used around lamps to direct light into the actual LCD. Some foil materials absorb considerably more field energy than others, creating loss. Finally, displays supplied in metal enclosures tend to be lossy. The metal absorbs significant energy and an AC path to ground is unavoidable. Direct grounding of a metal enclosed display further increases losses. Some display manufacturers have addressed this issue by relieving the metal in the lamp area with other materials.

The highest efficiency "in system" backlights have been produced by careful attention to these issues. In some cases the entire display enclosure was re-engineered for lowest losses.

Layout Considerations for Two Lamp Designs

Systems using two lamps have some unique layout problems. Almost all two lamp displays are color units. The lower light transmission characteristics of color displays necessitates more light. As such, display manufacturers use two lamps to produce more light. The wiring layout of these two lamp color displays affects efficiency and illumination balance in the lamps. Figure 17 shows an "x-ray" view of a typical display. This symmetrical arrangement presents equal parasitic losses. If C1 and C2 and the lamps are matched, the circuit's current output splits evenly and equal illumination occurs.

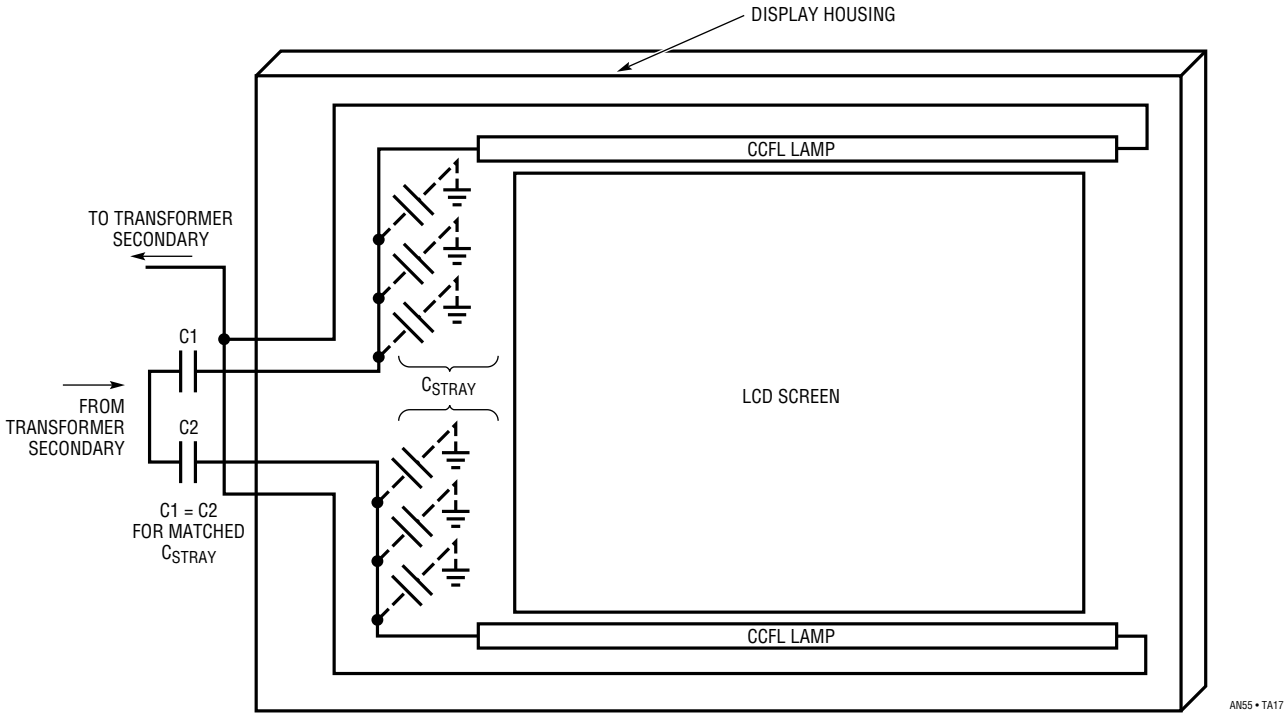

Figure 17. Loss Paths for a "Best Case" Dual Lamp Display. Symmetry Promotes Balanced Illumination

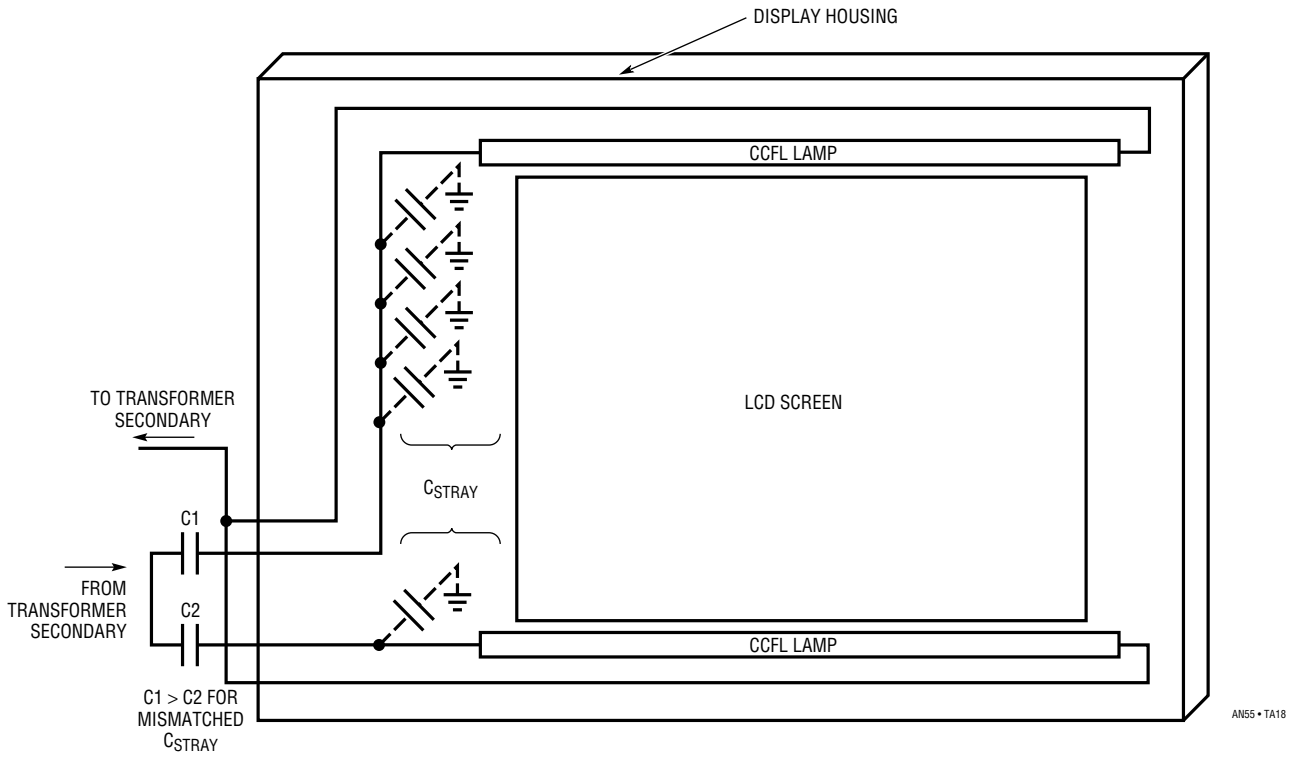

Figure 18. Asymetric Losses in a Dual Lamp Display. Skewing C1 and C2 Values Compensates Imbalanced Loss Paths, but Not Wasted Energy

Figure 18's display arrangement is less friendly. The asymmetrical wiring forces unequal losses, and the lamps receive imbalanced current. Even with identical lamps, illumination may not be balanced. This condition is correctable by skewing C1 and C2's values. C1, because it drives greater parasitic capacitance, should be larger than C2. This tends to equalize the currents, promoting equal lamp drive. It is important to realize that this compensation does nothing to recapture the lost energy—efficiency is still compromised. There is no substitute for minimizing loss paths.

In general, imbalanced illumination causes fewer problems than might be supposed. The effect is very difficult for the eye to detect at high intensity levels. Unequal illumination is much more noticeable at lower levels. In the worst case the dimmer lamp may only partially illuminate. This phenomenon, sometimes called "Thermometering," is discussed in detail in the text section "Extending Illumination Range."

Feedback Loop Stability Issues

The circuits shown to this point rely on closed loop feedback to maintain the operating point. All linear closed loop systems require some form of frequency compensation to achieve dynamic stability. Circuits operating with relatively low power lamps may be frequency compensated by simply overdamping the loop. Text Figures 6, 8 and 10 use this approach. The higher power operation associated with color displays requires more attention to loop response. The transformer produces much higher output voltages, particularly at start-up. Poor loop damping can allow transformer voltage ratings to be exceeded, causing arcing and failure. As such, higher power designs may require optimization of transient response characteristics.

Figure 19 shows the significant contributors to loop transmission in these circuits. The resonant Royer converter delivers information at about 50kHz to the lamp. This

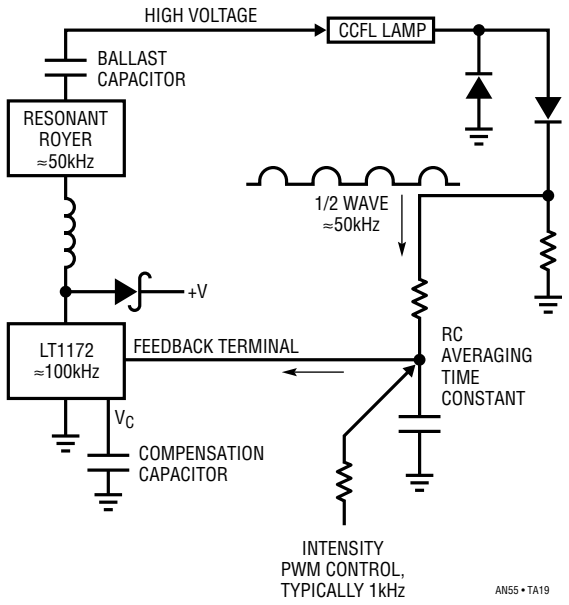

Figure 19. Delay Terms in the Feedback Path. The RC Time Constant Dominates Loop Transmission Delay and must be Compensated for Stable Operation

information is smoothed by the RC averaging time constant and delivered to the LT1172's feedback terminal as DC. The LT1172 controls the Royer converter at a 100kHz rate, closing the control loop. The capacitor at the LT1172 rolls off gain, nominally stabilizing the loop. This compensation capacitor must roll off the gain bandwidth at a low enough value to prevent the various loop delays from causing oscillation.

Which of these delays is the most significant? From a stability viewpoint the LT1172's output repetition rate and the Royer's oscillation frequency are sampled data systems. Their information delivery rate is far above the RC averaging time constants delay and is not significant. The RC time constant is the major contributor to loop delay. This time constant must be large enough to turn the half wave rectified waveform into DC. It also must be large enough to average any intensity control PWM signal to DC. Typically, these PWM intensity control signals come in at a 1kHz rate (see Appendix F, "Intensity Control and Shutdown Methods"). The RC's resultant delay dominates loop transmission. It must be compensated by the capacitor at the LT1172. A large enough value for this capacitor rolls off loop gain at low enough frequency to provide stability. The loop simply does not have enough gain to oscillate at a frequency commensurate with the RC delay.[10]

This form of compensation is simple and effective. It ensures stability over a wide range of operating conditions. It does, however, have poorly damped response at system turn-on. At turn-on the RC lag delays feedback, allowing output excursions well above the normal operating point. When the RC acquires the feedback value the loop stabilizes properly. This turn-on overshoot is not a concern if it is well within transformer breakdown ratings. Color displays, running at higher power, usually require large initial voltages. If loop damping is poor, the overshoot may be dangerously high. Figure 20 shows such a loop responding to turn-on. In this case the RC values are 10k and 4.7μF, with a 2μF compensation capacitor. Turn-on overshoot exceeds 3500V for over 10ms! Ring-off takes over 100ms before settling occurs. Additionally, an inadequate (too small) ballast capacitor and excessively lossy layout force a 2000V output once loop settling occurs. This photo was taken with a transformer rated well below this figure. The resultant arcing caused transformer destruction, resulting in field failures. A typical destroyed transformer appears in Figure 21.

Figure 22 shows the same circuit, with the RC values reduced to 10k and 1μF. The ballast capacitor and layout have also been optimized. Figure 22 shows peak voltage

Note 10: The high priests of feedback refer to this as "Dominant Pole Compensation." The rest of us are reduced to more pedestrian descriptives.

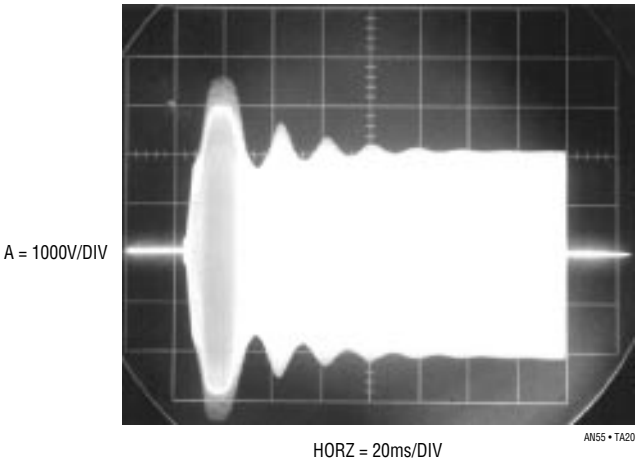

Figure 20. Destructive High Voltage Overshoot and Ring-Off Due to Poor Loop Compensation. Transformer Failure and Field Recall are Nearly Certain. Job Loss may also Occur

Figure 21. Poor Loop Compensation Caused this Transformer Failure. Arc Occured in High Voltage Secondary (Lower Right). Resultant Shorted Turns Caused Overheating

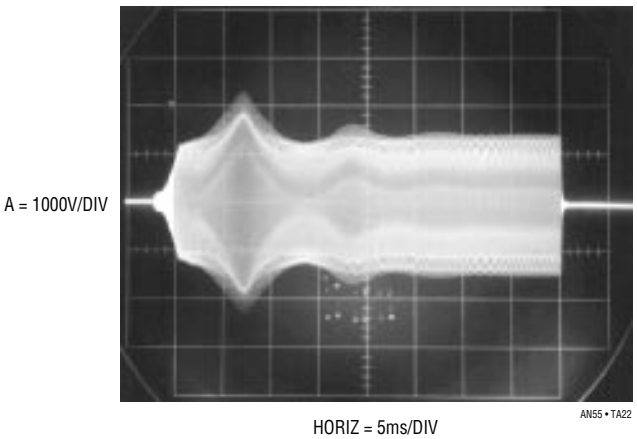

Figure 22. Reducing RC Time Constant Improves Transient Response, although Peaking, Ring-Off and Run Voltage are Still Excessive

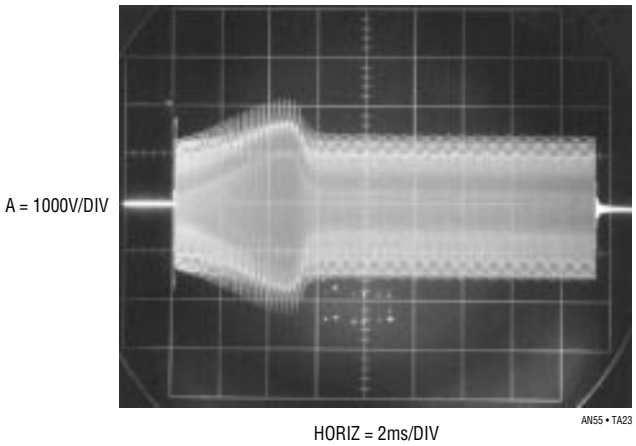

Figure 23. Additional Optimization of RC Time Constant and Compensation Capacitor Reduces Turn-On Transient. Run Voltage is Large, Indicating Possible Lossy Layout and Display

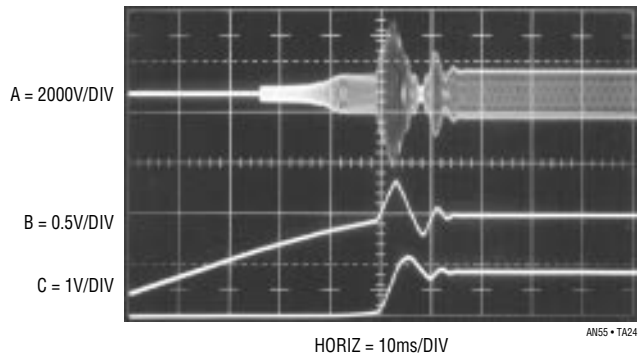

Figure 24. Waveforms for a Lower Loss Layout and Display. High Voltage Overshoot (Trace A) is Reflected at Compensation Node (Trace B) and Feedback Pin (Trace C)

reduced to 2.2kV with duration down to about 2ms (note horizontal scale change). Ring-off is also much quicker, with lower amplitude excursion. Increased ballast capacitor value and wiring layout optimization reduce running voltage to 1300V. Figure 23's results are even better. Changing the compensation capacitor to a 3kΩ-2μF network introduces a leading response into the loop, allowing faster acquisition. Now, turn-on excursion is slightly lower, but greatly reduced in duration (again, note horizontal scale change). The running voltage remains the same.

The photos show that changes in compensation, ballast value and layout result in dramatic reductions in overshoot amplitude and duration. Figure 20's performance almost guarantees field failures, while Figures 22 and 23 do not overstress the transformer. Even with the improvements, more margin is possible if display losses can be controlled. Figures 20-23 were taken with an exceptionally lossy display. The metal enclosure was very close to the metallic foil wrapped lamps, causing large losses with subsequent high turn-on and running voltages. If the display is selected for lower losses, performance can be greatly improved.

Figure 24 shows a low loss display responding to turn-on with a 2μF compensation capacitor and 10k-1μF RC values. Trace A is the transformer's output while Traces B and C are the LT1172's $V_{Compensation}$ and feedback pins, respectively. The output overshoots and rings badly,

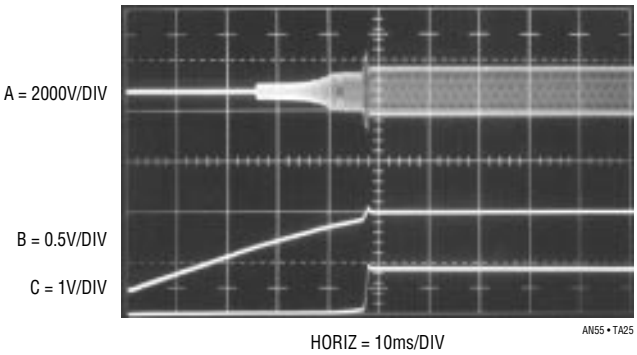

Figure 25. Reducing RC Time Constant Produces Quick, Clean Loop Behavior. Low Loss Layout and Display Result in 650V_{RMS} Running Voltage

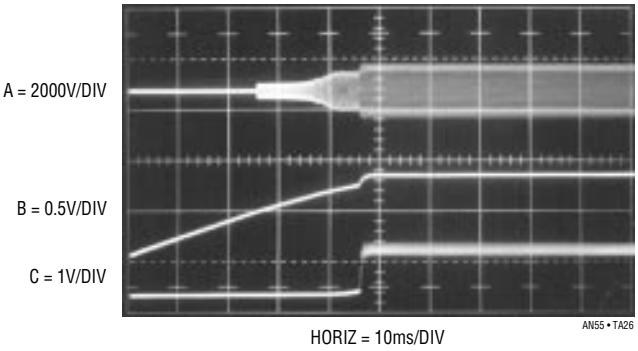

Figure 26. Very Low RC Value Provides Even Faster Response, but Ripple at Feedback Pin (Trace C) is too High. Figure 25 is the Best Compromise

peaking to about 3000V. This activity is reflected by overshoots at the $V_{Compensation}$ pin (the LT1172's error amplifier output) and the feedback pin. In Figure 25 the RC is reduced to 10kΩ-0.1μF. This substantially reduces loop delay. Overshoot goes down to only 800V—a reduction of almost a factor of four. Duration is also much shorter. The $V_{Compensation}$ and feedback pins reflect this tighter control. Damping is much better, with slight overshoot induced at turn-on. Further reduction of the RC to 10k-0.01μF (Figure 26) results in even faster loop capture, but a new problem appears. In Trace A lamp turn on is so fast the overshoot does not register in the photo. The $V_{Compensation}$ (Trace B) and feedback nodes (Trace C) reflect this with exceptionally fast response. Unfortunately, the RC's light filtering causes ripple to appear when the feedback node settles. As such, Figure 25's RC values are probably more realistic for this situation.

The lesson from this exercise is clear. The higher voltages involved in color displays mandate attention to transformer outputs. Under running conditions layout and display losses can cause higher loop compliance voltages, degrading efficiency and stressing the transformer. At turn-on improper compensation causes huge overshoots, resulting in possible transformer destruction. Isn't a day of loop and layout optimization worth a field recall?

Extending Illumination Range

Lamps operating at relatively low currents may display the "thermometer effect," that is, light intensity may be non-uniformly distributed along lamp length. Figure 27 shows that although lamp current density is uniform, the associated field is imbalanced. The field's low intensity, combined with its imbalance, means that there is not enough energy to maintain uniform phosphor glow beyond some point. Lamps displaying the thermometer effect emit most of their light near the positive electrode, with rapid emission fall-off as distance from the electrode increases. Placing a conductor along the lamp's length largely alleviates "thermometering." The trade-off is decreased efficiency due to energy leakage (see footnote 8 and associated text). It is worth noting that various lamp types have different degrees of susceptibility to the thermometer effect.

Some displays require extended illumination range. "Thermometering" usually limits the lowest practical illumination level. One acceptable way to minimize "thermometering" is to eliminate the large field imbalance. Figure 28's circuit does this. This circuit's most significant

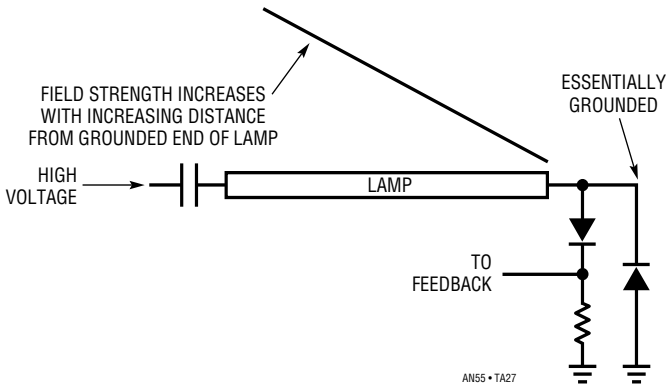

Figure 27. Field Strength vs Distance for a Ground Referred Lamp. Field Imbalance Promotes Uneven Illumination at Low Drive Levels

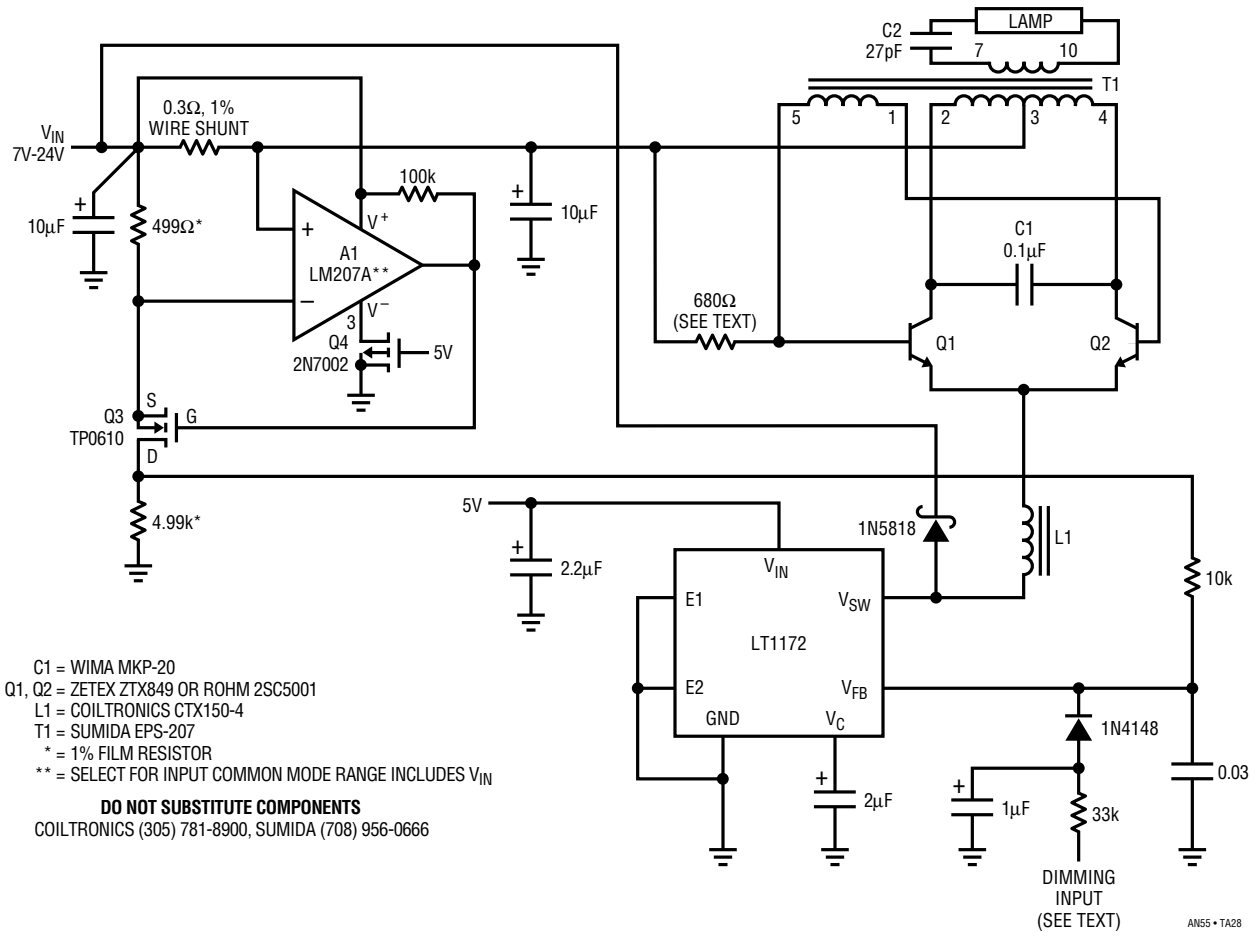

Figure 28. The "Low Thermometer" Configuration. "Topside Sensed" Primary Derived Feedback Balances Lamp Drive, Extending Dimming Range

aspect is that the lamp is fully floating—there is no galvanic connection to ground as in the previous designs. This allows T1 to deliver symmetric, differential drive to the lamp. Such balanced drive eliminates field imbalance, reducing thermometering at low lamp currents. This approach precludes any feedback connection to the now floating output. Maintaining closed loop control necessitates deriving a feedback signal from some other point. In theory, lamp current proportions to T1's or L1's drive level, and some form of sensing this can be used to provide feedback. In practice, parasitics make a practical implementation difficult.[11]

Figure 28 derives the feedback signal by measuring Royer converter current and feeding this information back to the LT1172. The Royer's drive requirement closely proportions to lamp current under all conditions. A1 senses this current across the 0.3Ω shunt and biases Q3, closing a local feedback loop. Q3's drain voltage presents an amplified, single ended version of the shunt voltage to the feedback point, closing the main loop. The lamp current is not as tightly controlled as before, but 0.5% regulation over wide supply ranges is possible. The dimming in this circuit is controlled by a 1kHz PWM signal. Note the heavy filtering (33k-1µF) *outside* the feedback loop. This allows a fast time constant, minimizing turn-on overshoot.[12]

In all other respects operation is similar to the previous circuits. This circuit typically permits the lamp to operate over a 40:1 intensity range without "thermometering." The normal feedback connection is usually limited to a 10:1 range.

Note 11: See Appendix J, "A Lot of Cut-Off Ears and No Van Goghs—Some Not-So-Great Ideas," for details.

Note 12: See text section, "Feedback Loop Stability Issues."

The losses introduced by the current shunt and A1 degrade overall efficiency by about 2%. As such, circuit efficiency is limited to about 90%. Most of the loss can be recovered at moderate cost in complexity. Figure 29's modifications reduce shunt and A1 losses. A1, a precision micropower type, cuts power drain and permits a smaller shunt value without performance degradation. Unfortunately, A1 does not function when its inputs reside at the V^+ rail. Because the circuit's operation requires this, some accommodation must be made.[13]

At circuit start-up A1's input is pulled to its supply pin potential (actually, slightly above it). Under these conditions A1's input stage is shut off. Normally, A1's output state would be indeterminate but, for the amplifier specified, it will always be high. This turns off Q3, permitting the LT1172 to drive the Royer stage. The Royer's operation causes Q1's collector swing to exceed the supply rail. This turns on the 1N4148, the BAT-85 goes off and A1's supply pin rises above the supply rail. This "bootstrapping" action results in A1's inputs being biased within the amplifier's common mode range and normal circuit operation commences.

The result of all this is a 1.6% efficiency gain, permitting an overall circuit efficiency of just below 92%.

Note 13: In other words, we need a hack.

Synchronizing

In some situations it is desirable to synchronize circuit operation to a system clock. In particular, pen based computers may be especially sensitive to asynchronous components. The LT1172 can be synchronized by briefly pulling its V_C pin to ground (see LT1172 data sheet).

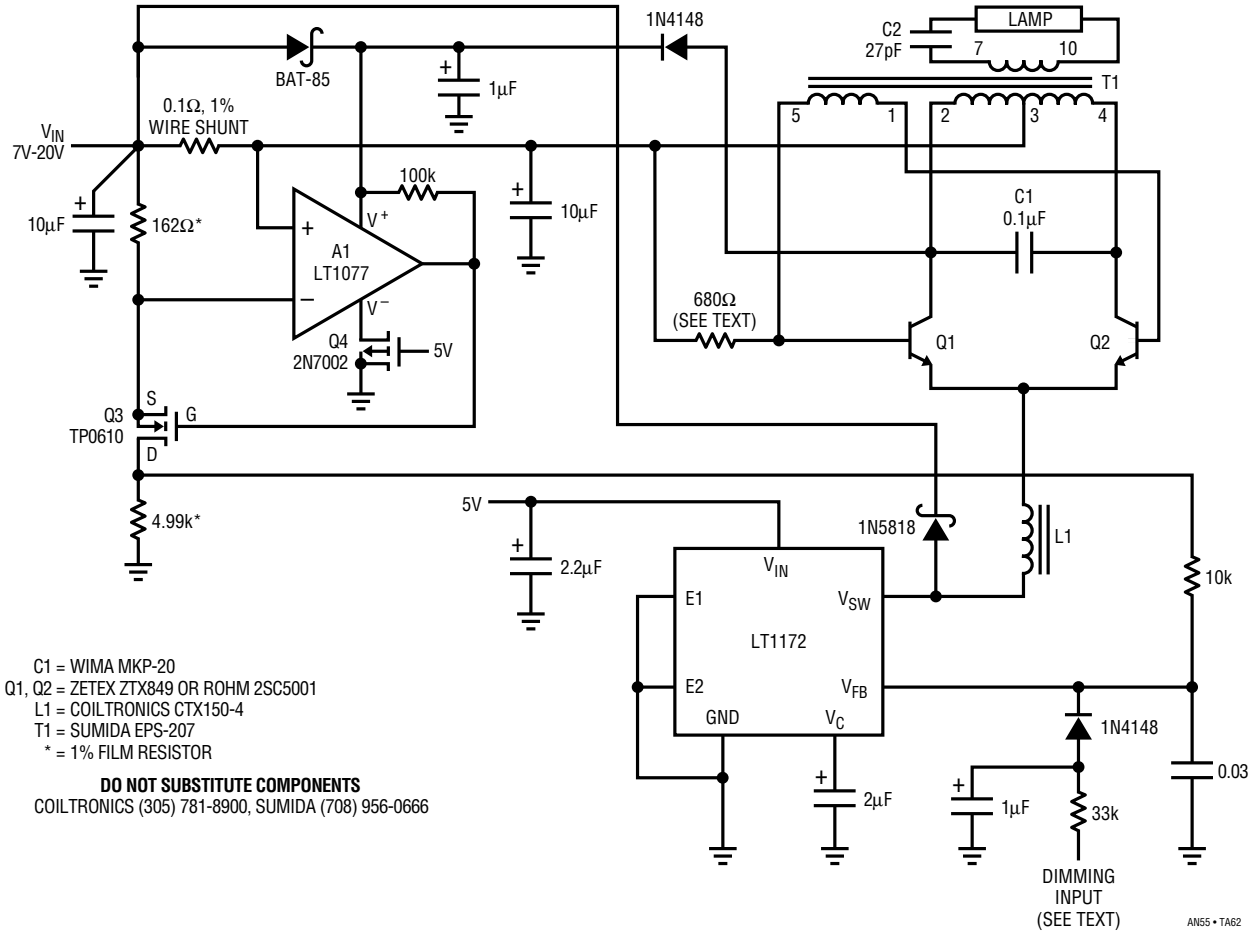

Figure 29. The "Low Thermometer" Circuit using a Micropower, Precision Topside Sensing Amplifier. Supply Bootstrapping Eliminates Input Common Mode Requirement, Permitting a 1.6% Efficiency Gain

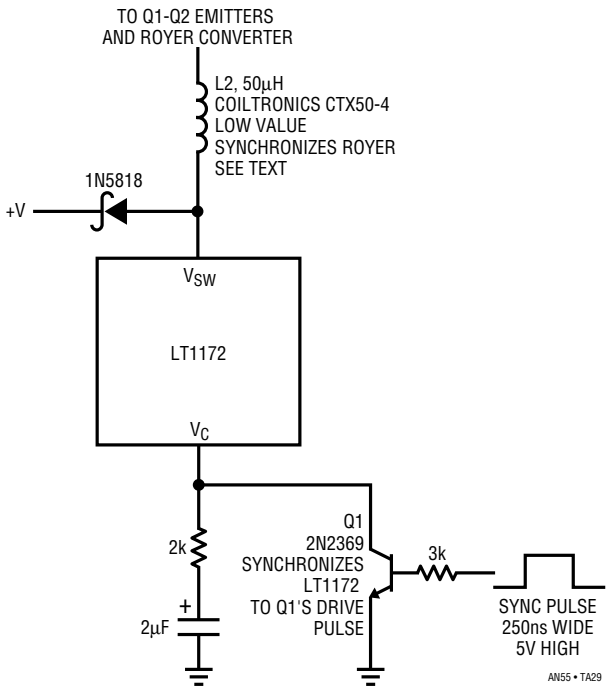

Figure 30. Synchronizing by Lowering L2's Value

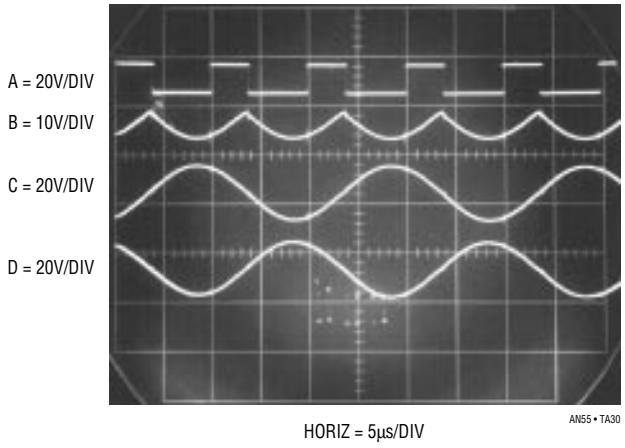

Figure 31. Waveforms for Synchronized Operation

Figure 30 shows a way to do this via Q1 and associated components. If Royer synchronization is also required, reducing L2's value can do this under some conditions. L2's low value introduces greater LT1172 harmonic, causing the Royer to lock at 1/2 the LT1172's switching frequency. This can only occur *if the free running Royer frequency is close to this value.* Pulling the Royer away from its resonant frequency causes some efficiency loss. A further limitation is that, although synchronization is never lost, phase jitter increases over extended dimming and supply ranges. Typically, 2.5:1 ranges of supply and 10:1 dimming range are practical. Efficiency is typically degraded by about 5% at full power. This approach to full synchronization is simple, but interactions are complex and require careful evaluation for any specific application. Figure 31 shows LT1172 V_{SW} pin, Q1-Q2 emitter and Royer collector waveforms (Traces A, B, C and D respectively) for a synchronized circuit.

Figure 32 uses a different approach to achieve fully synchronized operation. Here, Q1 and Q2 are driven from L3. L3's drive, in turn, comes from a flip-flop which is clocked from the LT1172's V_{SW} pin. L3 provides a level shift, allowing drive to the floating Q1-Q2 pair. The flip-flop's differential drive prevents DC biasing of L3. D1 and D2 permit L3's output current to alternately bias Q1 and Q2 without V_{BE} reverse bias occurring. Figure 33 shows operating waveforms. Trace A is the LT1172 V_{SW} pin while traces B and C are the flip-flop outputs. Traces D and E are the Q1-Q2 bases and Traces F and G their collectors. This scheme works reasonably well, although phase jitter and

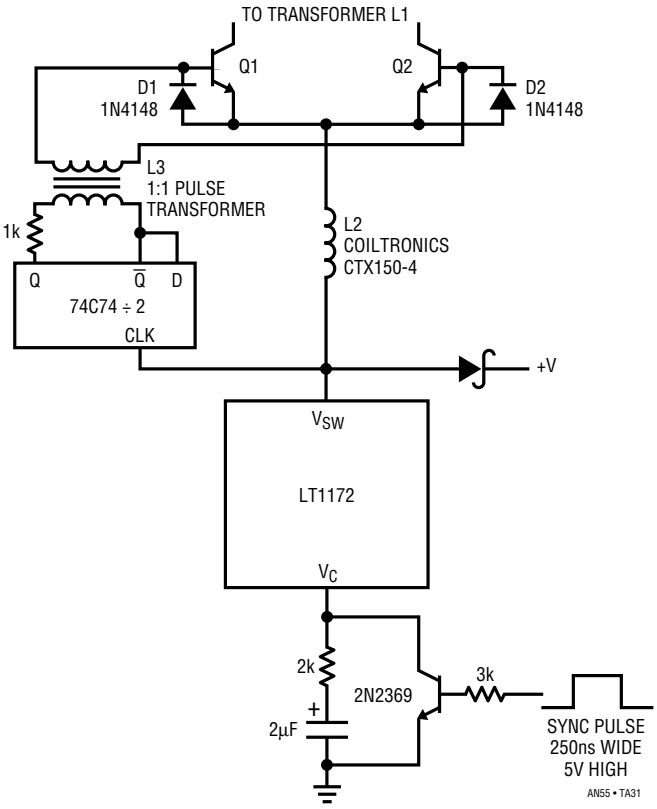

Figure 32. Synchronizing by Driving the DC to AC Converter

efficiency restrictions (similar to those previously described) apply.

Figure 34's approach eliminates phase jitter. This prototype circuit replaces the Royer configuration with a flip-flop driven pair, Q1-Q2. The flip-flop is driven from an external clock. This clock also sets the frequency of the step-down regulator feeding the L1 based high voltage converter. The step-down regulator supplies a DC potential to L2. L2's "output" end sources current to the L1 based converter. C1, C2, L1 and the lamp form a tank circuit which, nominally, resonates at the clock regulated frequency. L1's high voltage output puts current through the lamp. Feedback from the lamp, similar to the previous circuit's, closes a control loop at the step-down regulator. The 0.22µF capacitor stabilizes this loop.

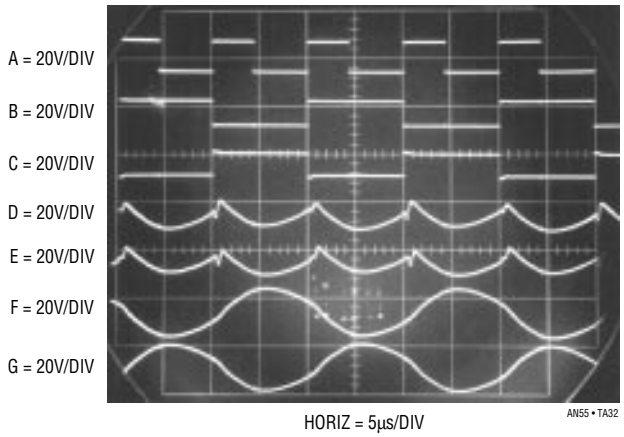

Figure 33. Waveforms for the Driven DC to AC Converter

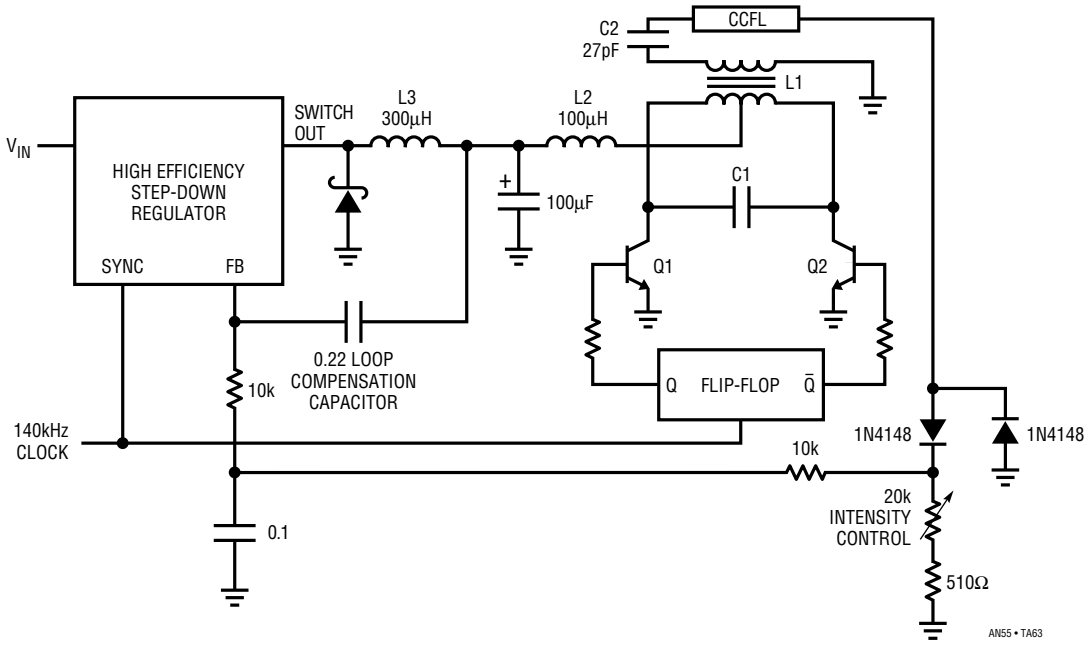

Figure 34. An Inherently Synchronous CCFL Circuit Eliminates Phase Jitter. Trade-Offs Include Increased Complexity and Lower Efficiency over Lamp Operating Range

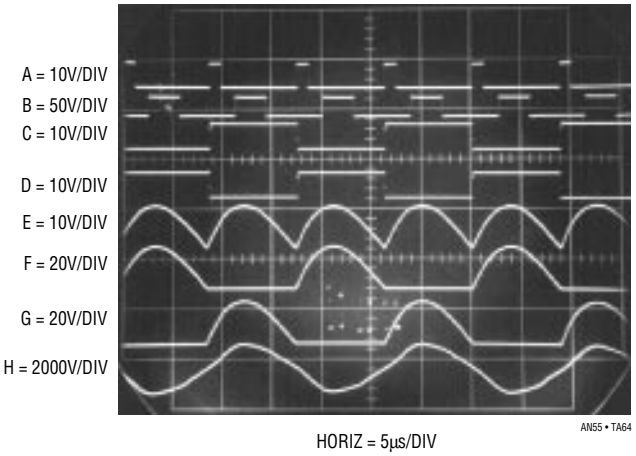

Figure 35. The Fully Synchronized CCFL Circuit's Waveforms, Taken During On-Resonance Operation

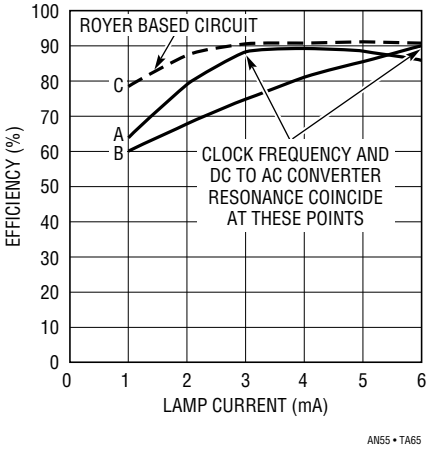

Figure 36. Efficiency vs Lamp Current for the Synchronous Circuit. Off-Resonance Operation Causes Efficiency Fall-Off away from Indicated Lamp Currents

Figure 35 shows circuit waveforms. Trace A is the clock, while Trace B is the step-down regulator's switch output. Traces C and D are flip-flop Q and $\overline{Q}$ outputs, respectively. Trace E is the L2-L1 junction and Traces F and G are the Q1 and Q2 collectors, respectively. Trace H is L1's high voltage output. The waveforms show that the synchronous drive to the resonant high voltage converter produces a clean sine wave output. The driven, fully synchronous operation eliminates phase jitter under all conditions. This circuit has the same excellent power supply rejection and regulation characteristics of the Royer based approach.

A potential drawback to this approach is that the resonant frequency of the high voltage converter changes with lamp operating current. The Royer based circuits inherently change frequency in response to this, maintaining on-resonance operation. This contributes to high efficiency operation over a broad range of lamp currents. This circuit's fixed frequency drive means that on-resonance operation only occurs at one lamp current. In practice, C1 and C2 set the "true" resonant operating point at any desired current. Efficiency falls off at other currents because the high voltage converter is forced to run off-resonance.

Figure 36's plot shows the effects of this on efficiency. Curve A results with the circuit optimized at 3mA lamp current (1/2 power), while Curve B represents optimization at 6mA (full power). In both cases, efficiency suffers at currents away from these points. Curve C shows a Royer based circuit's performance for comparison.

The circuit is also sensitive to C1 and C2 tolerances. A 10% total tolerance deviation can cause 4% efficiency degradation at the nominally optimized current.

Note: *This application note was derived from a manuscript originally prepared for publication in EDN Magazine.*

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APPENDIX A

"HOT" CATHODE FLUORESCENT LAMPS

Many CCFL characteristics are shared by so-called "Hot" Cathode Fluorescent Lamps (HCFLs). The most significant difference is that HCFLs contain filaments at each end of the lamp (see Figure A1). When the filaments are powered they emit electrons, lowering the lamp's ionization potential. This means a significantly lower voltage will start the lamp. Typically the filaments are turned on, a relatively modest voltage impressed across the lamp, and start-up occurs. Once the lamp starts, filament power is removed. Although HCFLs reduce the high voltage requirement they require a filament supply and sequencing circuitry. The CCFL circuits shown in the text will start and run HCFLs without using the filaments. In practice this involves simply driving the filament connections at the HCFL ends as if they were CCFL electrodes.

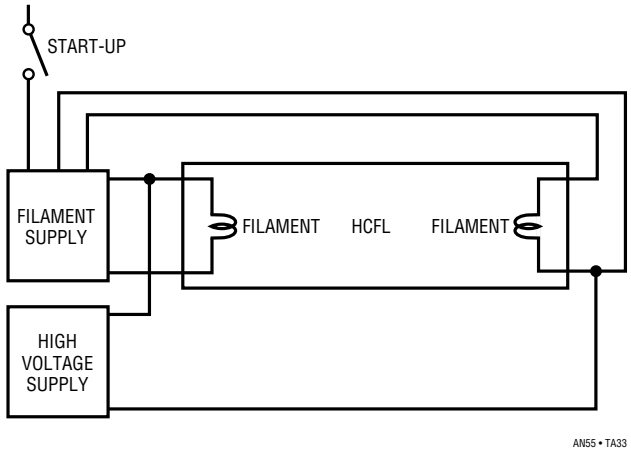


Figure A1. A Conceptual Hot Cathode Fluorescent Lamp Power Supply. Heated Filaments Liberate Electrons, Lowering the Lamp's Start-Up Voltage Requirement. CCFL Supply Discussed in Text Eliminates Filament Supply

APPENDIX B

MECHANICAL DESIGN CONSIDERATIONS FOR LIQUID CRYSTAL DISPLAYS

Charles L. Guthrie, Sharp Electronics Corporation

Introduction

As more companies begin the manufacturing of their next generation of computers, there is a need to reduce the overall size and weight of the units to improve their portability. This has sparked the need for more compact designs where the various components are placed in closer proximity, thus making them more susceptible to interaction from signal noise and heat dissipation. The following is a summary of guidelines for the placement of the display components and suggestions for overcoming difficult design constraints associated with component placement.

In notebook computers the thickness of the display housing is important. The design usually requires the display to be in a pivotal structure so that the display may be folded down over the keyboard for transportation. Also, the outline dimensions must be minimal so that the package will remain as compact as possible. These two constraints drive the display housing design and placement of the display components. This discussion surveys each of the problems facing the designer in detail and offers suggestions for overcoming the difficulties to provide a reliable assembly.

The problems facing the pen based computer designer are similar to those realized in notebook designs. In addition, however, pen based designs require protection for the face of the display. In pen based applications, as the pen is moved across the surface of the display, the pen has the potential for scratching the front polarizer. For this reason the front of the display must be protected. Methods for protecting the display face while minimizing effects on the display image are given.

Additionally, the need to specify the flatness of the bezel is discussed. Suggestions for acceptable construction techniques for sound design are included. Further, display components likely to cause problems due to heat buildup are identified and methods for minimization of the heat's effects are presented.

The ideas expressed here are not the only solutions to the various problems and have not been assessed as to whether they may infringe on any patents issued or applied for.

Flatness and Rigidity of the Bezel

In the notebook computer the bezel has several distinct functions. It houses the display, the inverter for the backlight, and in some instances, the controls for contrast and brightness of the display. The bezel is usually designed to tilt to set the optimum viewing angle for the display.

It is important to understand that the bezel must provide a mechanism to keep the display flat, particularly at the mounting holds. Subtle changes in flatness place uneven stress on the glass which can cause variations in contrast across the display. Slight changes in pressure may cause significant variation in the display contrast. Also, at the extreme, significantly uneven pressures can cause the display glass to fail.

Because the bezel must be functional in maintaining the flatness of the display, consideration must be made for the strength of the bezel. Care must be taken to provide structural members, while minimizing the weight of the unit. This may be executed using a parallel grid, normal to the edges of the bezel, or angled about 45° off of the edges of the bezel. The angled structure may be more desirable in that it provides resistance to torquing the unit while lifting the cover with one hand. Again, the display is sensitive to stresses from uneven pressure on the display housing.

Another structure which will provide excellent rigidity, but adds more weight to the computer, is a "honeycomb" structure. This "honeycomb" structure resists torquing from all directions and tends to provide the best protection for the display.

With each of these structures it is easy to provide mounting assemblies for the display. "Blind nuts" can be molded into the housing. The mounting may be done to either the front or rear of the bezel. Attachment to the rear may provide better rigidity for placement of the mounting hardware.

One last caution is worth noting in the development of a bezel. The bezel should be engineered to absorb most of the shock and vibration experienced in a portable computer. Even though the display has been carefully designed, the notebook computer presents extraordinary shock and abuse problems.

Avoiding Heat Buildup in the Display

Several of the display components are sources for heat problems. Thermal management must be taken into account in the design of the display bezel. A heated display may be adversely affected; a loss of contrast uniformity usually results. The Cold Cathode Fluorescent Tube (CCFT) itself gives off a small amount of heat relative to the amount of power dissipated in its glow discharge. Likewise, even though the inverters are designed to be extremely efficient, there is some heat generated. The buildup of heat in these components will be aggravated by the typically "tight" designs currently being introduced. There is little ventilation designed into most display bezels. To compound the problem, the plastics used are poor thermal conductors, thus causing the heat to build up which may affect the display.

Some current designs suffer from poor placement of the inverter and/or poor thermal management techniques. These designs can be improved, even where redesign of the display housing, with improved thermal management, is impractical.

One of the most common mistakes in current designs is that there has been no consideration for the buildup of heat from the CCFT. Typically, the displays for notebook applications have only one CCFT to minimize display power requirements. The lamp is usually placed along the right edge of the display. Since the lamp is placed very close to the display glass, it can cause a temperature rise in the liquid crystal. It is important to note that variations in temperature of as little as 5°C can cause an apparent nonuniformity in display contrast. Variations caused by slightly higher temperature variations will cause objectionable variations in the contrast and display appearance.

To further aggravate the situation, some designs have the inverter placed in the bottom of the bezel. This has a tendency to cause the same variations in contrast, particularly when the housing does not have any heat sinking for the inverter. This problem manifests itself as a "blooming" of the display, just above the inverter. This "blooming"

looks like a washed out area where, in the worst case, the characters on the display fade completely.

The following section discusses the recommended methods for overcoming these design problems.

Placement of the Display Components

One of the things that can be done is to design the inverter into the base of the computer with the motherboard. In some applications this is impractical because this requires the high voltage leads to be mounted within the hinges connecting the display bezel to the main body. This causes a problem with strain relief of the high voltage leads, and thus with UL certification.

One mistake, made most often, is placing the inverter at the bottom of the bezel next to the lower edge of the display. It is a fact that heat rises, yet this is one of the most overlooked problems in new notebook designs. Even though the inverters are very efficient, some energy is lost in the inverter in the form of heat. Because of the insulating properties of the plastic materials used in the bezel construction, heat builds up and affects the display contrast.

Designs with the inverter at the bottom can be improved in one of three ways. The inverter can be relocated away from the display, heat sinking materials can be placed between the display and the inverter, or ventilation can be provided to remove the heat.

In mature designs, it may be impractical to do what is obvious and move the inverter up to the side of the display towards the top of the housing. In these cases, the inverter may be insulated from the display with a "heat dam." One method of accomplishing this would be to use a piece of mica insulator die cut to fit tightly between the inverter and the display. This heat dam would divert the heat around the end of the display bezel to rise harmlessly to the top of the housing. Mica is recommended in this application because of it's thermal and electrical insulation properties.

The last suggestion for removing heat is to provide some ventilation to the inverter area. This has to be done very carefully to prevent exposing the high voltage. Ventilation may not be a practical solution because resistance to liquids and dust is compromised.

The best solution for the designer of new hardware is to consider the placement of the inverter to the side of the display and at the top of the bezel. In existing designs of this type the effects of heat from the inverter, even in tight housings, has been minimal or non-existent.

One problem which is aggravated by the placement of the inverter at the bezel is heat dissipated by the CCFT. In designs where the inverter is placed up and to the side of the display, fading of the display contrast due to CCFT heat is not a problem. However, when the inverter is placed at the bezel bottom, some designs experience a loss of contrast aggravated by the heat from the CCFT and inverter.

In cases where the inverter must be left at the bottom, and the CCFT is causing a loss of contrast, the problem can be minimized by using an aluminum foil heat sink. This does not remove the heat from the display, but dissipates it over the entire display area, thus normalizing the display contrast. The aluminum foil is easy to install and in some present designs has successfully improved the display contrast.

Remember that the objection to the contrast variation stems more from non-uniformity than from a total loss of contrast.

Protecting the Face of the Display

One of the last considerations in the design of notebook and pen based computers is protection of the display face. The front polarizer is made of a mylar base and thus is susceptible to scratching. The front protection for the display, along with providing scratch protection, may also provide an anti-glare surface.

There are several ways that scratch resistance and anti-glare surfaces can be incorporated. A glass or plastic cover may be placed over the display, thus providing protection. The material should be placed as close to the display as possible to minimize possible parallax problems due to reflections off of the cover material. With anti-glare materials, the further the material is from the front of the display the greater the distortion.

In pen applications, the front anti-scratch material is best placed in contact with the front glass of the display. The cover glass material normally needs to be slightly thicker

to protect the display from distortion when pressure is being exerted on the front.

There are several methods for making the pen input devices. Some use the front surface of the cover glass to provide input data and some use a field effect to a printed wiring board on the back of the display. When the pen input is on the front of the display, the input device is usually on a glass surface.

To limit specular reflection in this application, the front cover glass should be bonded to the display. Care must be taken to insure that the coefficient of thermal expansion is matched for all of the materials used in the system. Because of the difficulties encountered with the bonding of the cover glass, and the potential to destroy the display through improper workmanship, consulting an expert is strongly recommended.

APPENDIX C

ACHIEVING MEANINGFUL EFFICIENCY MEASUREMENTS

Obtaining reliable efficiency data for the CCFL circuits presents a high order difficulty measurement problem. Establishing and maintaining accurate AC measurements is a textbook example of attention to measurement technique. The combination of high frequency, harmonic laden waveforms and high voltage makes meaningful results difficult to obtain. The choice, understanding and use of test instrumentation is crucial. Clear thinking is needed to avoid unpleasant surprises![1]

Probes

The probes employed must faithfully respond over a variety of conditions. Measuring across the resistor in series with the CCFL is the most favorable circumstance. This low voltage, low impedance measurement allows use of a standard 1X probe. The probe's relatively high input capacitance does not introduce significant error. A 10X probe may also be used, but frequency compensation issues (discussion to follow) must be attended to.

The high voltage measurement across the lamp is considerably more demanding on the probe. The waveform fundamental is at 20kHz to 100kHz, with harmonics into the MHz region. This activity occurs at peak voltages in the kilovolt range. The probe must have a high fidelity response under these conditions. Additionally, the probe should have low input capacitance to avoid loading effects which would corrupt the measurement. The design and construction of such a probe requires significant attention. Figure C1 lists some recommended probes along with their characteristics. As stated in the text, almost all standard oscilloscope probes *will fail* [2] if used for this measurement. Attempting to circumvent the probe requirement by resistively dividing the lamp voltage also creates problems. Large value resistors often have significant voltage coefficients and their shunt capacitance is high and uncertain. As such, simple voltage dividing is not recommended. Similarly, common high voltage probes intended for DC measurement will have large errors because of AC effects. The P6013A and P6015 are the favored probes; their 100MΩ input and small capacitance introduces low loading error. The penalty for their 1000X attenuation is reduced output, but the recommended voltmeters (discussion to follow) can accommodate this.

All of the recommended probes are designed to work into an oscilloscope input. Such inputs are almost always 1MΩ paralleled by (typically) 10pF-22pF. The recommended voltmeters, which will be discussed, have significantly different input characteristics. Figure C2's table shows higher input resistances and a range of capacitances. Because of this the probe must be compensated for the voltmeter's input characteristics. Normally, the optimum compensation point is easily determined and adjusted by observing probe output on an oscilloscope. A known amplitude square wave is fed in (usually from the oscilloscope calibrator) and the probe adjusted for correct response. Using the probe with the voltmeter presents an unknown impedance mismatch and raises the problem of determining when compensation is correct.

Note 1: It is worth considering that various constructors of text Figure 6 have reported efficiencies ranging from 8% to 115%.

Note 2: That's twice we've warned you nicely.

TEKTRONIX PROBE TYPE	ATTENUATION FACTOR	ACCURACY	INPUT RESISTANCE	INPUT CAPACITANCE	RISE TIME	BAND-WIDTH	MAXIMUM VOLTAGE	DERATED ABOVE	DERATED TO AT FREQUENCY	COMPENSATION RANGE	ASSUMED TERMINATION RESISTANCE
P6007	100X	3%	10MΩ	2.2pF	14ns	25MHz	1.5kV	200kHz	$700V_{RMS}$ at 10MHz	15-55pF	1M
P6009	100X	3%	10MΩ	2.5pF	2.9ns	120MHz	1.5kV	200kHz	$450V_{RMS}$ at 40MHz	15-47pF	1M
P6013A	1000X	Adjustable	100MΩ	3pF	7ns	50MHz	12kV	100kHz	$800V_{RMS}$ at 20MHz	12-60pF	1M
P6015	1000X	Adjustable	100MΩ	3pF	4.7ns	75MHz	20kV	100kHz	$2000V_{RMS}$ at 20MHz	12-47pF	1M

Figure C1. Characteristics of some Wideband High Voltage Probes. Output Impedances are Designed for Oscilloscope Inputs

MANUFACTURER AND MODEL	FULL SCALE RANGES	ACCURACY AT 1MHz	ACCURACY AT 100kHz	INPUT RESISTANCE AND CAPACITANCE	MAXIMUM BANDWIDTH	CREST FACTOR
Hewlett-Packard 3400 Meter Display	1mV to 300V, 12 Ranges	1%	1%	0.001V to 0.3V Range = 10M and < 50pF, 1V to 300V Range = 10M and < 20pF	10MHz	10:1 At Full Scale, 100:1 At 0.1 Scale
Hewlett-Packard 3403C Digital Display	10mV to 1000V, 6 Ranges	0.5%	0.2%	10mV and 100mV Range = 20M and 20pF ±10%, 1V to 1000V Range = 10M and 24pF ±10%	100MHz	10:1 At Full Scale, 100:1 At 0.1 Scale
Fluke 8920A Digital Display	2mV to 700V, 7 Ranges	0.7%	0.5%	10M and < 30pF	20MHz	7:1 At Full Scale, 70:1 At 0.1 Scale

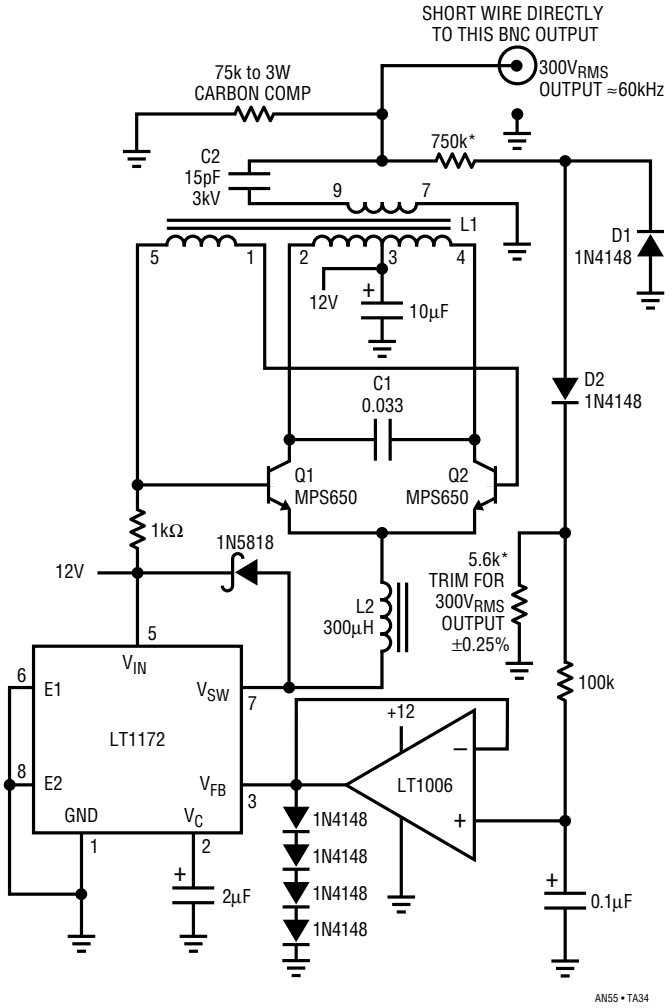
Figure C2. Pertinent Characteristics of some Thermally Based RMS Voltmeters. Input Impedances Necessitate Matching Network and Compensation for High Voltage Probes

The impedance mismatch occurs at low and high frequency. The low frequency term is corrected by placing an appropriate value resistor in shunt with the probe's output. For a 10MΩ voltmeter input a 1.1MΩ resistor is suitable. This resistor should be built into the smallest possible BNC equipped enclosure to maintain a coaxial environment. No cable connections should be employed; the enclosure should be placed *directly* between the probe output and the voltmeter input to minimize stray capacitance. This arrangement compensates the low frequency impedance mismatch. Figure C4 shows the impedance matching box attached to the high voltage probe.

Correcting the high frequency mismatch term is more involved. The wide range of voltmeter input capacitances combined with the added shunt resistor's effects presents problems. How is the experimenter to know where to set the high frequency probe compensation adjustment? One solution is to feed a known value RMS signal to the probe-voltmeter combination and adjust compensation for a proper reading. Figure C3 shows a way to generate a known RMS voltage. This scheme is simply a standard backlight circuit reconfigured for a constant voltage output. The op amp permits low RC loading of the 5.6k feedback termination without introducing bias current error. The 5.6kΩ value may be series or parallel trimmed for a 300V output. Stray parasitic capacitance in the feedback network affects output voltage. Because of this, all feedback associated nodes and components should be rigidly fixed and the entire circuit built into a small metal box. This prevents any significant change in the parasitic terms. The result is a known $300V_{RMS}$ output.

Now, the probe's compensation is adjusted for a 300V voltmeter indication using the shortest possible connection (e.g., BNC-to-probe adapter) to the calibrator box. This procedure, combined with the added resistor, completes the probe-to-voltmeter impedance match. If the probe compensation is altered (e.g., for proper response on an oscilloscope) the voltmeter's reading will be erroneous.[3] It is good practice to verify the calibrator box output before and after every set of efficiency measurements. This is done by *directly* connecting, via BNC adapters, the calibrator box to the RMS voltmeter on the 1000V range.

Note 3: The translation of this statement is to hide the probe when you are not using it. If anyone wants to borrow it, look straight at them, shrug your shoulders and say you don't know where it is. This is decidedly dishonest, but eminently practical. Those finding this morally questionable may wish to re-examine their attitude after producing a day's worth of worthless data with a probe that was unknowingly readjusted.



C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 OR MKP-20 (GERMAN) RECOMMENDED
L1 = SUMIDA 6345-020 OR COILTRONICS CTX110092-1
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = COILTRONICS CTX300-4
Q1, Q2 = AS SHOWN OR BCP 56 (PHILLIPS SO PACKAGE)
* = 1% FILM RESISTOR (TEN 75kΩ RESISTORS IN SERIES)
DO NOT SUBSTITUTE COMPONENTS

COILTRONICS (305) 781-8900, SUMIDA (708) 956-0666

Figure C3. High Voltage RMS Calibrator is Voltage Output Version of CCFL Circuit

RMS Voltmeters

The efficiency measurements require an RMS responding voltmeter. This instrument must respond accurately at high frequency to irregular and harmonically loaded waveforms. These considerations eliminate almost all AC voltmeters, including DVMs with AC ranges.

There are a number of ways to measure RMS AC voltage. Three of the most common include *average, logarithmic,*

Figure C4. The Impedance Matching Box (Extreme Left) Mated to the High Voltage Probe. Note Direct Connection. No Cable is used

and *thermally* responding. Averaging instruments are calibrated to respond to the average value of the input waveform, which is almost always assumed to be a sine wave. Deviation from an ideal sine wave input produces errors. Logarithmically based voltmeters attempt to overcome this limitation by continuously computing the input's true RMS value. Although these instruments are "real time" analog computers their 1% error bandwidth is well below 300kHz and crest factor capability is limited. Almost all general purpose DVMs use such a logarithmically based approach and, as such, are not suitable for CCFL efficiency measurements. Thermally based RMS voltmeters are direct acting thermo-electronic analog computers. They respond to the input's RMS heating value. This technique is explicit, relying on the very definition of RMS (e.g., the heating power of the waveform). By turning the input into heat, thermally based instruments achieve vastly higher bandwidth than other techniques.[4] Additionally, they are insensitive to waveform shape and easily accommodate large crest factors. These characteristics are necessary for the CCFL efficiency measurements.

Figure C5 shows a conceptual thermal RMS-DC converter. The input waveform warms a heater, resulting in increased output from its associated temperature sensor. A DC amplifier forces a second, identical, heater-sensor pair to the same thermal conditions as the input driven pair. This differentially sensed, feedback enforced loop makes ambient temperature shifts a common mode term, eliminating their effect. Also, although the voltage and thermal interaction is nonlinear, the input-output RMS voltage relationship is linear with unity gain.

Note 4: Those finding these descriptions intolerably brief are commended to References 4, 5 and 6.

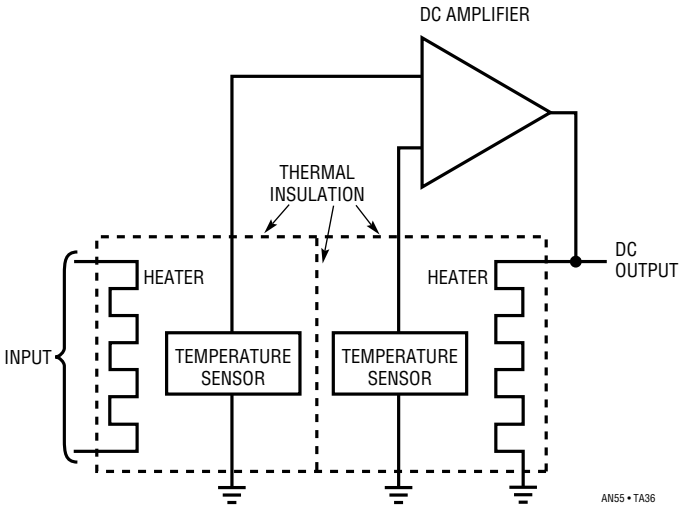


Figure C5. Conceptual Thermal RMS-DC Converter

The ability of this arrangement to reject ambient temperature shifts depends on the heater-sensor pairs being isothermal. This is achievable by thermally insulating them with a time constant well below that of ambient shifts. If the time constants to the heater-sensor pairs are matched, ambient temperature terms will affect the pairs equally in phase and amplitude. The DC amplifier rejects this common mode term. Note that, although the pairs are isothermal, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms. This would cause unfavorable signal-to-noise performance, limiting dynamic operating range.

Figure C5's output is linear because the matched thermal pair's nonlinear voltage-temperature relationships cancel each other.

The advantages of this approach have made its use popular in thermally based RMS-DC measurements.

The instruments listed in Figure C2, while considerably more expensive than other options, are typical of what is required for meaningful results. The HP3400A and the Fluke 8920A are currently available from their manufacturers. The HP3403C, an exotic and highly desirable instrument, is no longer produced but readily available on the secondary market.

Figure C6 shows equipment in a typical efficiency test set-up. The RMS voltmeters (photo center and left) read output voltage and current via high voltage (left) and standard 1X probes (lower left). Input voltage is read on a DVM (upper right). A low loss clip-on ammeter (lower right) determines input current. The CCFL circuit and LCD display are in the foreground. Efficiency, the ratio of input to output power, is computed with a hand held calculator (lower right).

Calorimetric Correlation of Electrical Efficiency Measurements

Careful measurement technique permits a high degree of confidence in the efficiency measurement's accuracy. It is, however, a good idea to check the method's integrity by measuring in a completely different domain. Figure C7 does this by calorimetric techniques. This arrangement, identical to the thermal RMS voltmeter's operation (Figure C5), determines power delivered by the CCFL circuit by measuring its load temperature rise. As in the thermal RMS voltmeter a differential approach eliminates ambient temperature as an error term. The differential amplifier's output, assuming a high degree of matching in the two thermal enclosures, proportions to load power. The ratio of the two cell's $E \times I$ products yields efficiency information. In a 100% efficient system the amplifier's output energy would equal the power supply's output. Practically it is always less, as the CCFL circuit has losses. This term represents the desired efficiency information.

Figure C8 is similar except that the CCFL circuit board is placed within the calorimeter. This arrangement nominally yields the same information, but is a much more demanding measurement because far less heat is generated. The signal-to-noise (heat rise above ambient) ratio is unfavorable, requiring almost fanatical attention to thermal and instrumentation considerations.[5] It is significant that the *total* uncertainty between electrical and both calorimetric efficiency determinations was 3.3%. The two thermal approaches differed by about 2%. Figure C9 shows the calorimeter and its electronic instrumentation. Descriptions of this instrumentation and thermal measurements can be found in the References section following the main text.

Note 5: Calorimetric measurements are not recommended for readers who are short on time or sanity.

AN55 • TA37

Figure C6. Typical Efficiency Measurement Instrumentation. RMS Voltmeters (Center Left) Measure Output Voltage and Current via Appropriate Probes. Clip-On Ammeter (Right) Gives Low Loss Input Current Readings. DVM (Upper Right) Measures Input Voltage. Hand Calculator (Lower Right) is used to Compute Efficiency

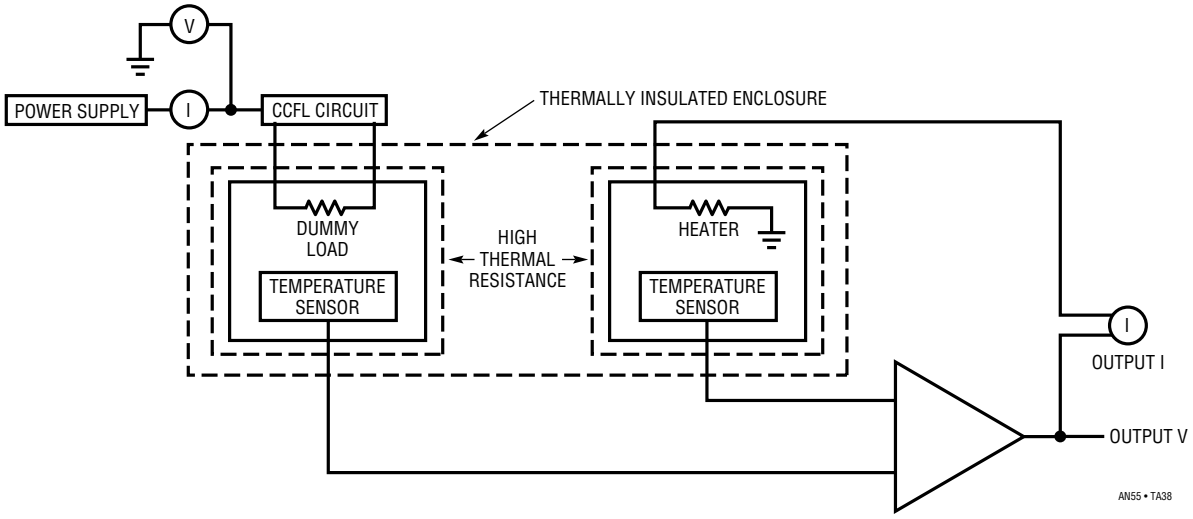


Figure C7. Efficiency Determination via Calorimetric Measurement. Ratio of Power Supply to Output Energy Gives Efficiency Information

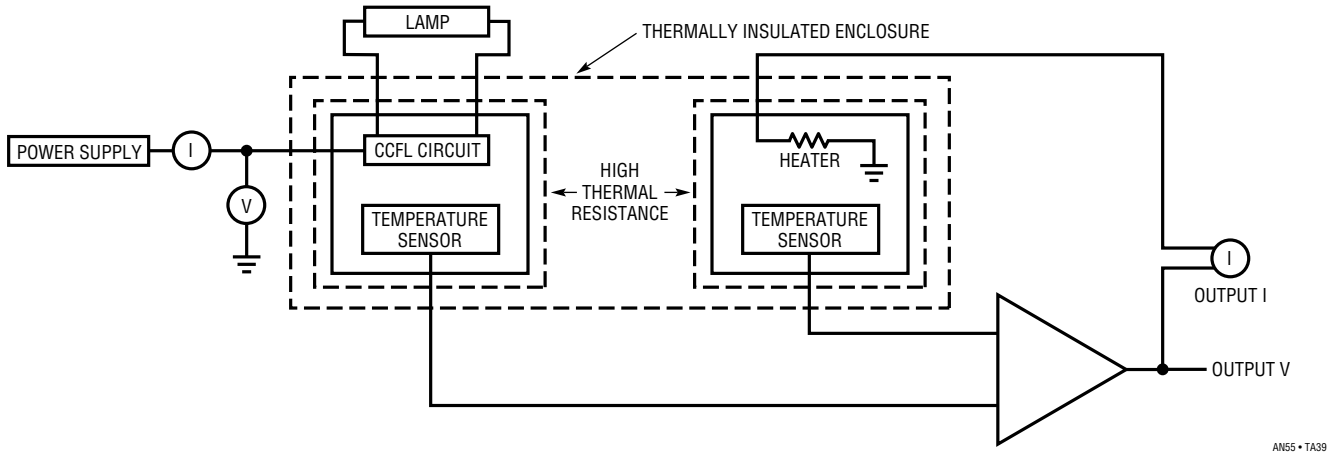


Figure C8. The Calorimeter Measures Efficiency by Determining Circuit Heating Losses

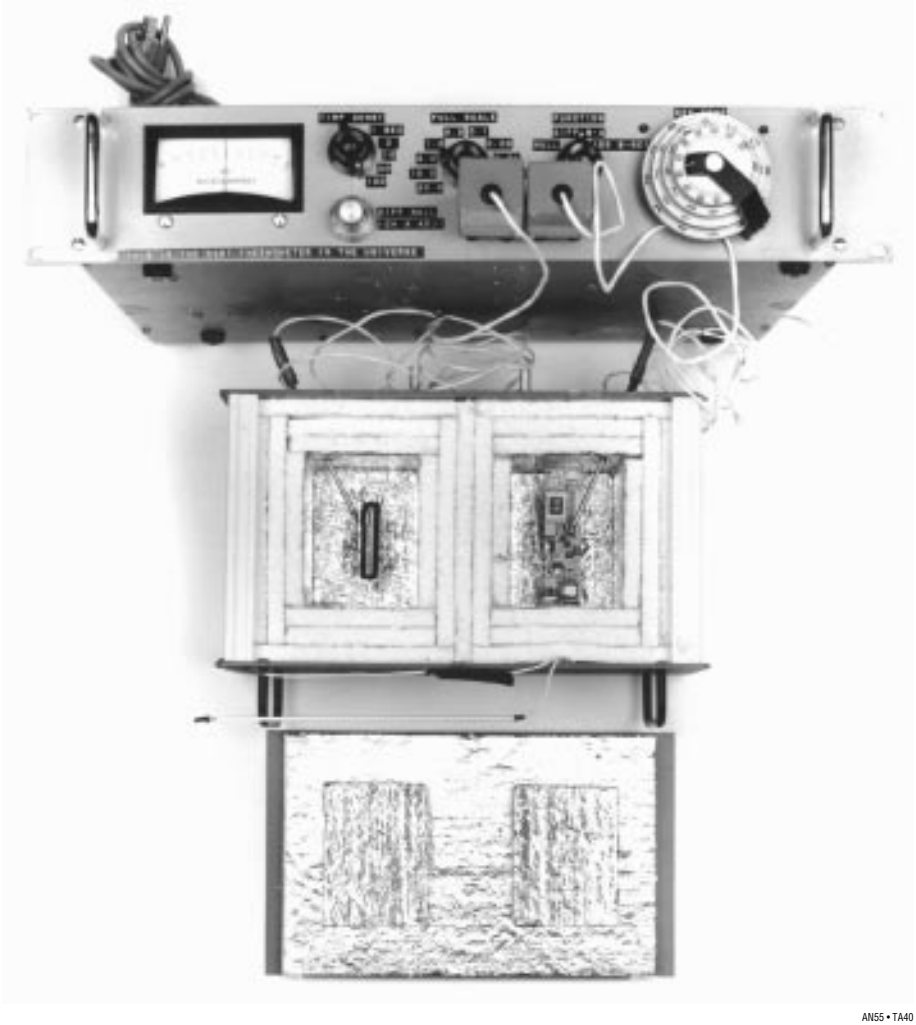


Figure C9. The Calorimeter (Center) and its Instrumentation (Top). Calorimeter's High Degree of Thermal Symmetry Combined with Sensitive Servo Instrumentation Produces Accurate Efficiency Measurements. Lower Portion of Photo is Calorimeter's Top Cover

APPENDIX D

PHOTOMETRIC MEASUREMENTS

In the final analysis, the ultimate concern centers around the efficient conversion of power supply energy to light. Emitted light varies monotonically with power supply energy,[1] but certainly not linearly. In particular, lamp luminosity may be highly nonlinear, particularly at high power, vs drive power. There are complex tradeoffs involving the amount of emitted light vs power consumption and battery life. Evaluating these tradeoffs requires some form of photometer. The relative luminosity of lamps may be evaluated by placing the lamp in a light tight tube and sampling its output with photodiodes. The photodiodes are placed along the lamp's length and their outputs electrically summed. This sampling technique is an uncalibrated measurement, providing relative data only. It is, however, quite useful in determining relative lamp emittance under various drive conditions. Figure D1 shows this "glometer," with its uncalibrated output appropriately scaled in "brights." The switches allow various sampling diodes along the lamp's length to be disabled. The photodiode signal conditioning electronics are mounted behind the switch panel.

Calibrated light measurements call for a true photometer. The Tektronix J-17/J1803 photometer is such an instrument. It has been found particularly useful in evaluating display (as opposed to simply the lamp) luminosity under various drive conditions. The calibrated output permits reliable correlation with customer results.[2] The light tight measuring head allows evaluation of emittance evenness at various display locations. This capability is invaluable when optimizing lamp location and/or ballast capacitor values in dual lamp displays.

Figure D2 shows the photometer in use evaluating a display.

Note 1: But not always! It is possible to build highly electrically efficient circuits that emit less light than "less efficient" designs. See Appendix J, "A Lot of Cut-Off Ears and No Van Goghs—Some Not-So-Great Ideas."

Note 2: It is unlikely customers would be enthusiastic about correlating the "brights" units produced by the aforementioned glometer.

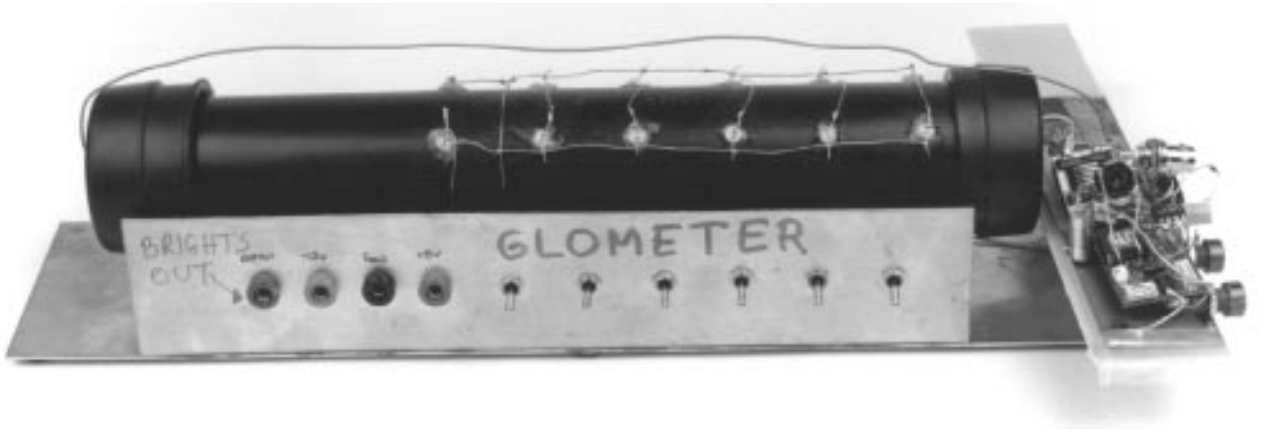


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Figure D1. The "Glometer" Measures Relative Lamp Emissivity. CCFL Circuit Mounts to the Right. Lamp is Inside Cylindrical Housing. Photodiodes (Center) Convert Light to Electrical Output (Lower Left) via Amplifiers (Not Visible in Photo)

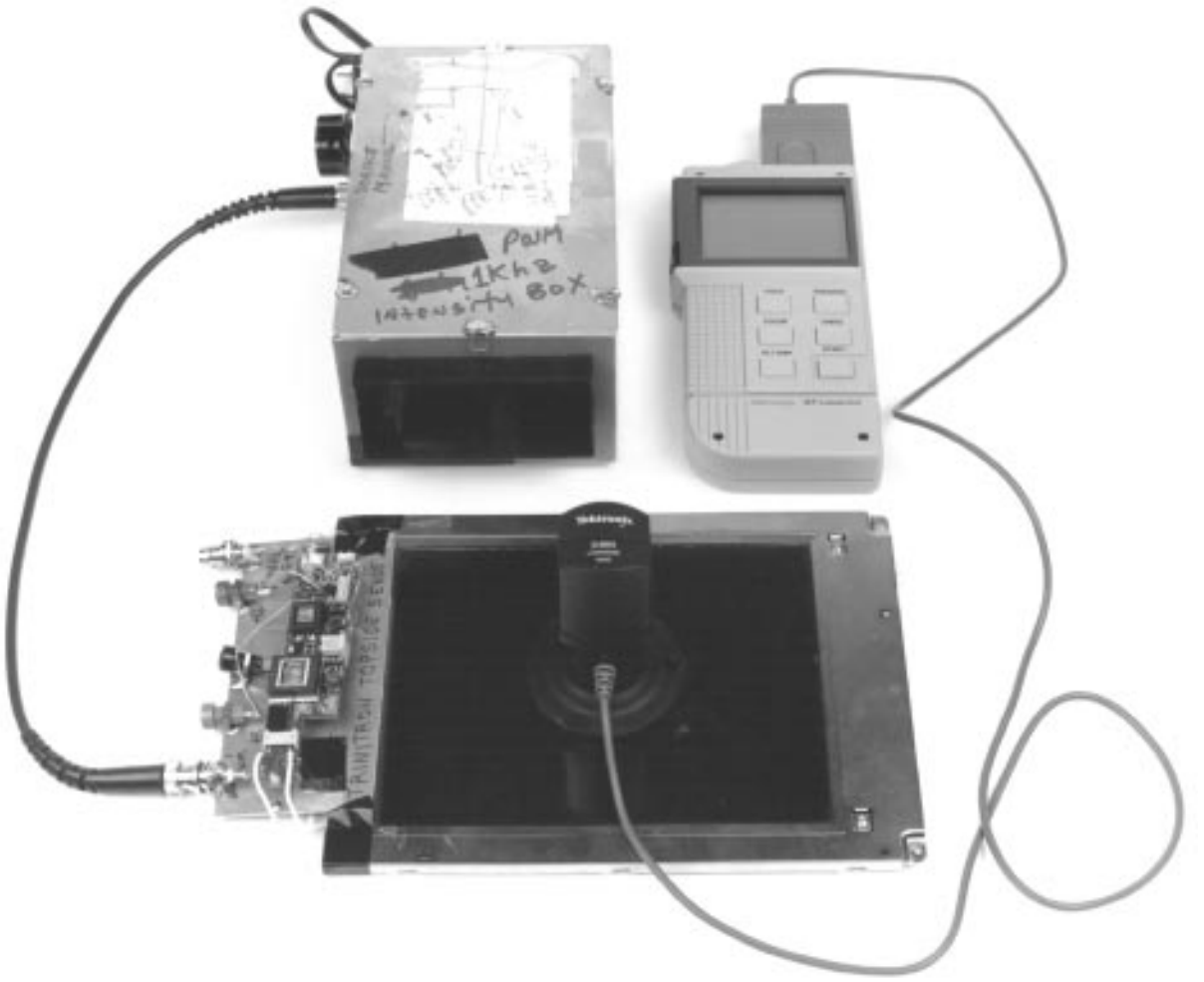

Figure D2. Apparatus for Calibrated Photometric Display Evaluation. Photometer (Upper Right) Indicates Display Luminosity via Sensing Head (Center). CCFL Circuit (Left) Intensity is Controlled by a Calibrated Pulse Width Generator (Upper Left)

APPENDIX E

OPEN LAMP PROTECTION

The CCFL circuit's current source output means that "open" or broken lamps cause full output voltage to appear. If this is objectionable Figure E1's modification may be employed. Q3 and associated components form a simple voltage mode feedback loop that operates if V_Z turns on. If T1 sees no load, there is no feedback and the Q1-Q2 pair receive full drive. Collector voltage rises to abnormal levels, and V_Z biases via Q1's V_{BE} path. Q1's collector current drives the feedback node and the circuit finds a stable operating point. This action controls Royer drive, and hence output voltage. Q3's sensing across the Royer provides power supply rejection. V_Z's value should be somewhat above the worst case Q1-Q2 V_{CE} voltage under running conditions. It is desirable to select V_Z's value so clamping occurs at the lowest output voltage possible while still permitting lamp start-up. This is not as tricky as it sounds because the 10k-1µF RC delays the effects of Q3's turn-on. Usually, selecting V_Z several volts above the worst case Q1-Q2 V_{CE} will suffice.

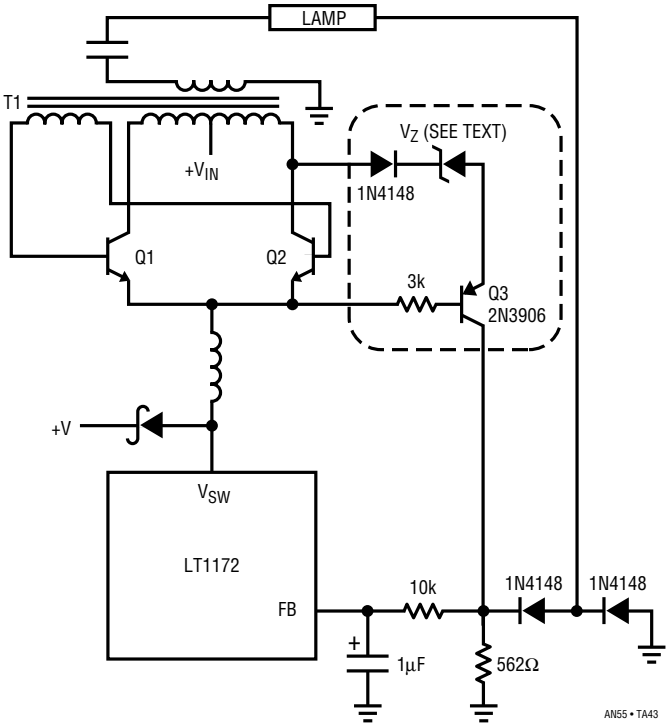

Figure E1. Q3 and Associated Components form a Local Regulating Loop to Limit Output Voltage

APPENDIX F

INTENSITY CONTROL AND SHUTDOWN METHODS

Figure F1 shows a variety of methods for shutting down and controlling intensity of the CCFL circuits. Pulling the LT1172 V_C pin to ground puts the circuit into micropower shutdown. In this mode about 50µA flows into the LT1172 V_{IN} pin with essentially no current drawn from the main (Royer center tap) supply. Turning off V_{IN} power eliminates the LT1172's 50µA drain.

Three basic ways to control intensity appear in the figure. The most common intensity control method is to add a potentiometer in series with the feedback termination. When using this method insure that the minimum value (in this case 562Ω) is a 1% unit. If a wider tolerance resistor is used the lamp current, at maximum intensity setting, will vary appropriately.

Pulse width modulation or variable DC is sometimes used for intensity control. Two interfaces work well. Directly driving the feedback pin via a diode—22k resistor with DC or PWM produces intensity control. The other method shown is similar, but places the 1µf capacitor outside the feedback loop to get best turn-on transient response. This is the best method if output overshoot must be minimized. See the main text section, "Feedback Loop Stability Issues" for pertinent discussion.

Figure F2 shows a simple circuit which generates precision variable pulse widths. This capability is useful when testing PWM based intensity schemes. The circuit is basically a closed loop pulse width modulator. The crystal controlled 1kHz input clocks the C1-Q1 ramp generator via

the differentiator—CMOS inverter network and the LTC201 reset switch. C1's output drives a CMOS inverter to furnish the output. The output is resistively sampled, averaged and presented to A1's negative input. A1 compares this signal with a variable voltage from the potentiometer. A1's output biases the pulse width modulator, closing a loop around it. The CMOS inverter's purely ohmic output structure combines with A1's ratiometric operation (e.g., both of A1's input signals derive from the +5V supply) to hold pulse width constant. Variations in time, temperature and supply have essentially no effect. The potentiometer's setting is the sole determinant of output pulse width. The Schottky diodes protect the output from latch-up due to cable induced ESD or accidental events[1] during testing.

The output width is calibrated by monitoring it with a counter while adjusting the 2kΩ trim pot.

As mentioned, the circuit is insensitive to power supply variation. However, the CCFL circuit averages the PWM output. It cannot distinguish between a duty cycle shift and supply variation. As such, the test box's 5V supply should be trimmed ±0.01V. This simulates a "design centered" logic supply under actual operating conditions. Similarly, paralleling additional logic inverters to get lower output impedance should be avoided. In actual use, the CCFL dimming port will be driven from a single CMOS output, and its impedance characteristics must be accurately mimicked.

Note 1: "Accidental events" is a nice way of referring to the stupid things we all do at the bench. Like shorting a CMOS logic output to a –15V supply (then I installed the diodes).

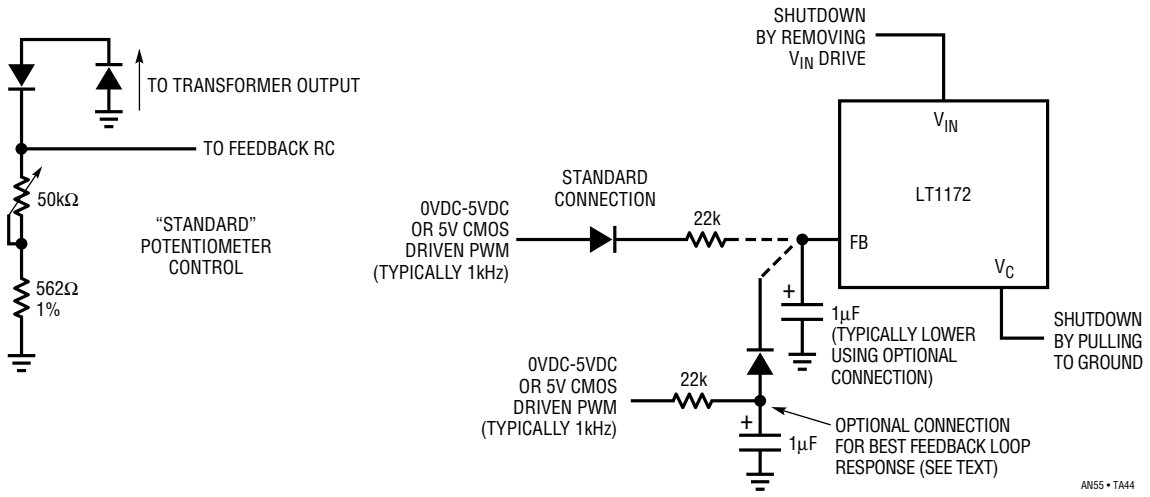

Figure F1. Various Options for Shutdown and Intensity Control

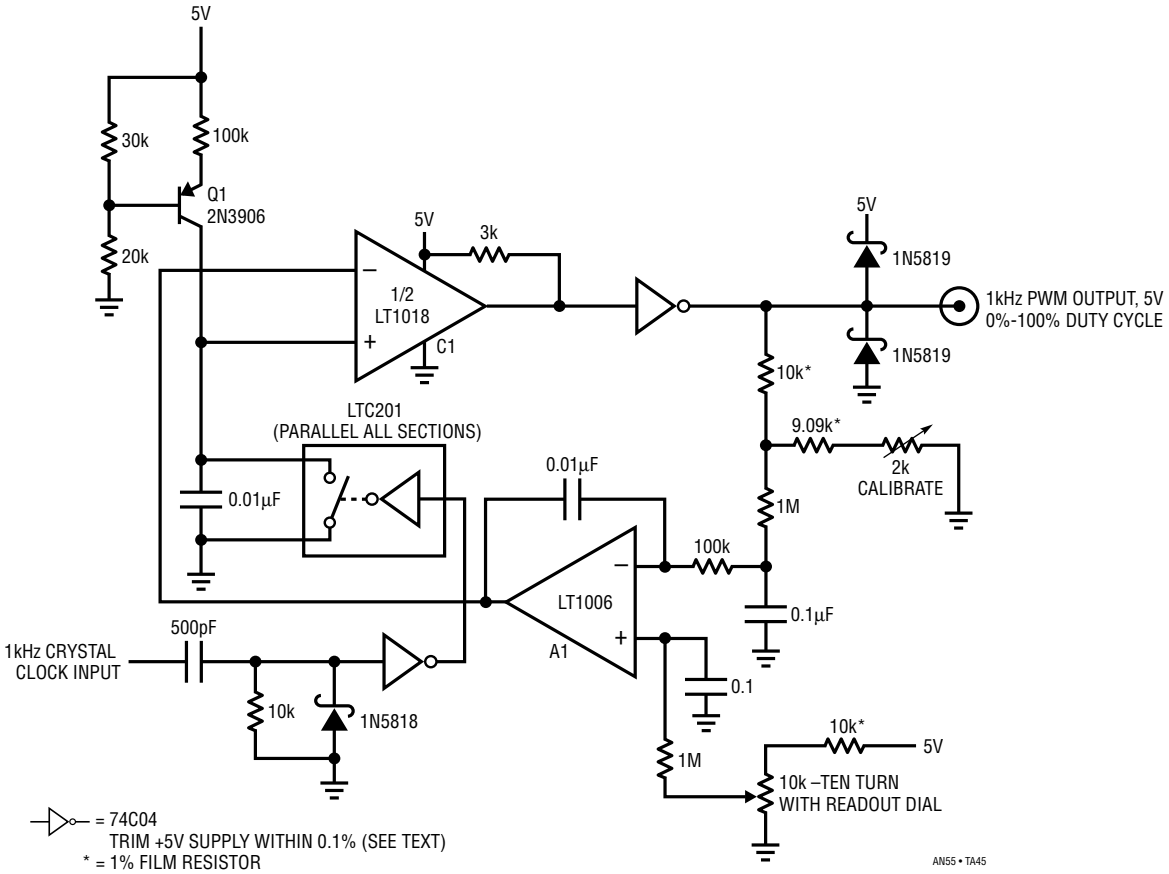

Figure F2. The Calibrated Pulse Width Test Box. A1 Controls C1 Based Pulse Width Modulator, Stabilizing its Operating Point

APPENDIX G

OPERATION FROM HIGH VOLTAGE INPUTS

Some applications require higher input voltages. The 20V maximum input specified in the figures is set by the LT1172 going into its isolated flyback mode (see LT1172 data sheet), not breakdown limits. If the LT1172 V_{IN} pin is driven from a low voltage source (e.g., 5V) the 20V limit may be extended by using Figure G1's network. If the LT1172 is driven from the same supply as L1's center tap, the network is unnecessary, although efficiency will suffer.

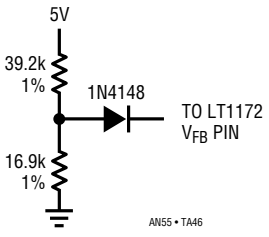

Figure G1. Network allows CCFL Operation beyond 20V Inputs

APPENDIX H

RELATED CIRCUITS

Higher Power Operation

There is no inherent limit on CCFL circuit output power. Figure H1's arrangement is a scaled up version of the text's CCFL circuits. This design, similar to ones employed for automotive use, drives a 25W CCFL. There are virtually no configuration changes, although most component power ratings have increased. The transistors can handle the higher currents, but all other power components are higher capacity. Efficiency is about 80%.

HeNe Laser Power Supply

Helium-neon lasers, used for a variety of tasks, are difficult loads for a power supply. They typically need almost 10kV to start conduction, although they require only about 1500V to maintain conduction at their specified operating currents. Powering a laser usually involves some form of start-up circuitry to generate the initial breakdown voltage and a separate supply for sustaining conduction. Figure H2's circuit considerably simplifies driving the laser. The start-up and sustaining functions have been combined into a single, closed-loop current source with over 10kV of compliance. The circuit is recognizable as a reworked CCFL power supply with a voltage tripled DC output.

When power is applied, the laser does not conduct and the voltage across the 190Ω resistor is zero. The LT1170 switching regulator FB pin sees no feedback voltage, and its switch pin (V_{SW}) provides full duty cycle pulse width modulation to L2. Current flows from L1's center tap through Q1 and Q2 into L2 and the LT1170. This current flow causes Q1 and Q2 to switch, alternately driving L1. The 0.47µF capacitor resonates with L1, providing boosted sine wave drive. L1 provides substantial step-up, causing about 3500V to appear at its secondary. The capacitors and diodes associated with L1's secondary form a voltage tripler, producing over 10kV across the laser. The laser breaks down and current begins to flow through it. The 47kΩ resistor limits current and isolates the laser's load characteristic. The current flow causes a voltage to appear across the 190Ω resistor. A filtered version of this voltage appears at the LT1170 FB pin, closing a control loop. The LT1170 adjusts pulse width drive to L2 to maintain the

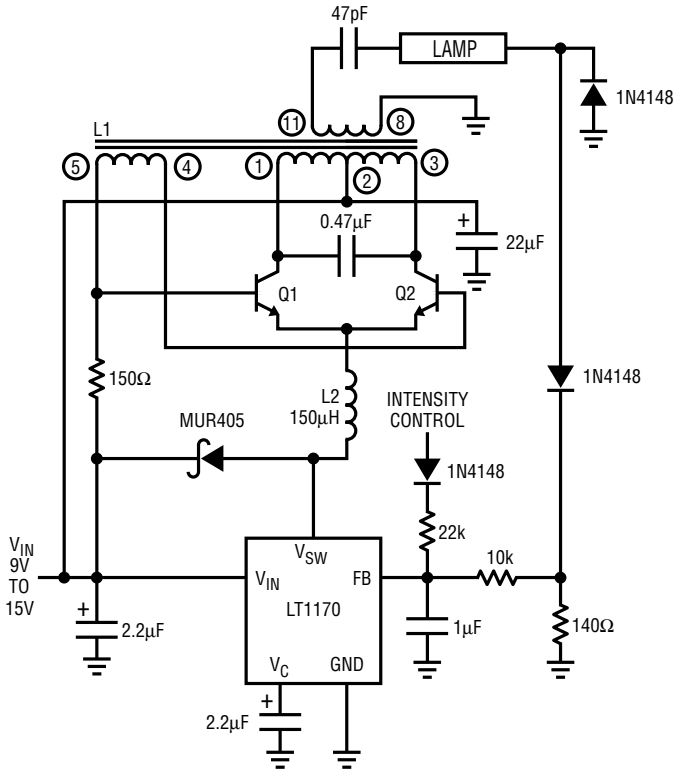

Figure H1. A 20W CCFL Supply

FB pin at 1.23V, regardless of changes in operating conditions. In this fashion, the laser sees constant current drive, in this case 6.5mA. Other currents are obtainable by varying the 190Ω value. The 1N4002 diode string clamps excessive voltages when laser conduction first begins, protecting the LT1170. The 10µF capacitor at the V_C pin frequency compensates the loop and the MUR405 maintains L1's current flow when the LT1170 V_{SW} pin is not conducting. The circuit will start and run the laser over a 9V-35V input range with an electrical efficiency of about 80%.

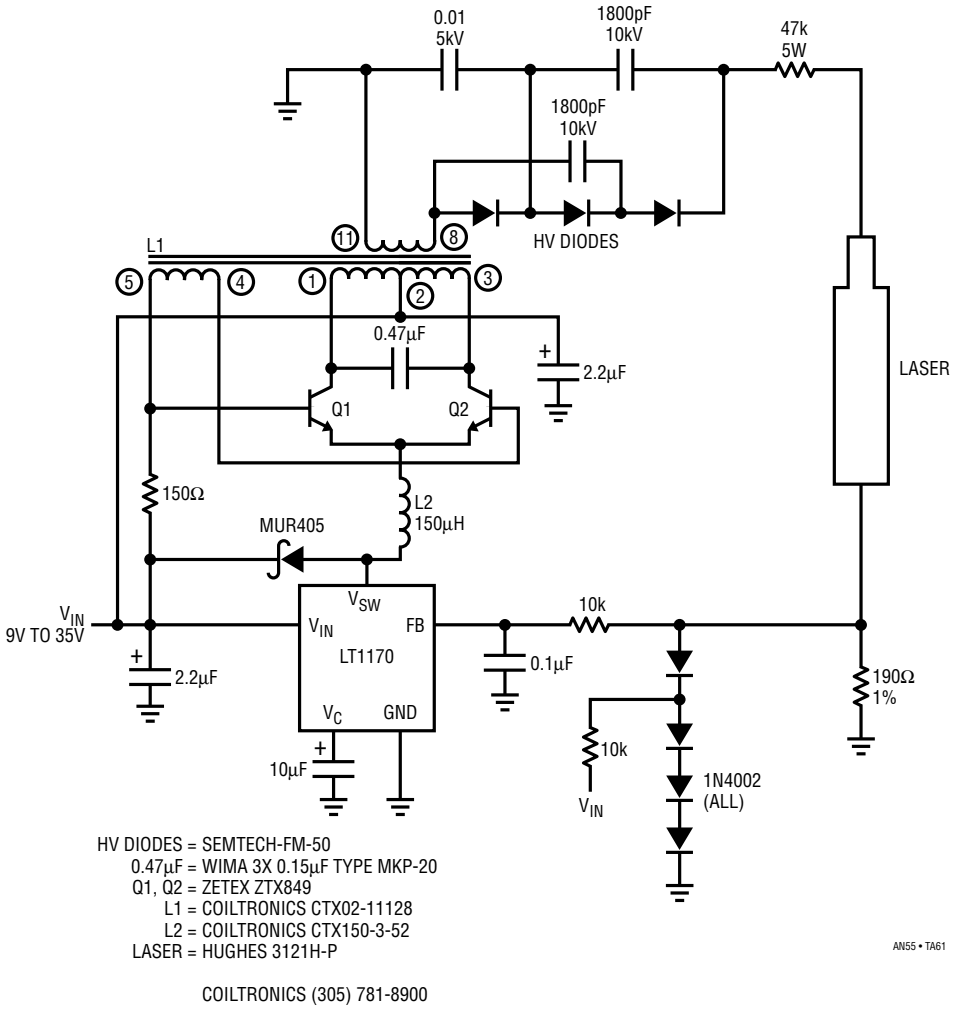

Figure H2. Laser Power Supply, Based on the CCFL Circuit, is Essentially a 10,000V Compliance Current Source

APPENDIX I

WHO WAS ROYER, AND WHAT DID HE DESIGN?

In December 1954 the paper "Transistors as On-Off Switches in Saturable-Core Circuits" appeared in *Electrical Manufacturing*. George H. Royer, one of the authors, described a "d-c to a-c converter" as part of this paper. Using Westinghouse 2N74 transistors, Royer reported 90% efficiency for his circuit. The operation of Royer's circuit is well described in this paper. The Royer converter was widely adopted, and used in designs from watts to kilowatts. It is still the basis for a wide variety of power conversion.

Royer's circuit is not an LC resonant type. The transformer is the sole energy storage element and the output is a square wave. Figure I1 is a conceptual schematic of a typical converter. The input is applied to a self-oscillating configuration composed of transistors, a transformer and a biasing network. The transistors conduct out of phase, switching (Figure I2, Traces A and C are Q1's collector and base, while Traces B and D are Q2's collector and base) each time the transformer saturates. Transformer saturation causes a quickly rising, high current to flow (Trace E).

This current spike, picked up by the base drive winding, switches the transistors. This phase opposed switching causes the transistors to exchange states. Current abruptly drops in the formerly conducting transistor and then slowly rises in the newly conducting transistor until saturation again forces switching. This alternating operation sets transistor duty cycle at 50%.

Photograph I3 is a time and amplitude expansion of I2's Traces B and E. It clearly shows the relationship between transformer current (Trace B, Figure I3) and transistor collector voltage (Trace A, Figure I3).[1]

Note 1: The bottom traces in both photographs are not germane and are not referenced in the discussion.

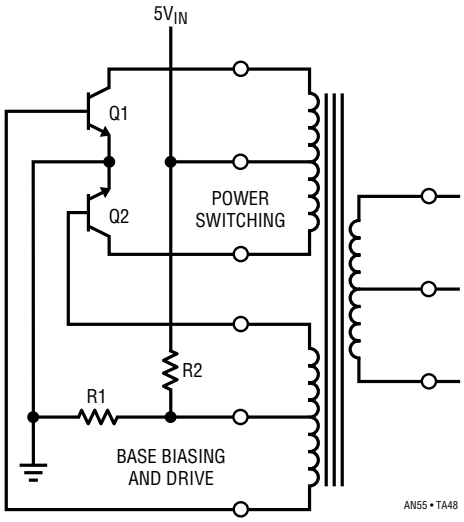

Figure I1. Conceptual Classic Royer Converter. Transformer Approaching Saturation Causes Switching

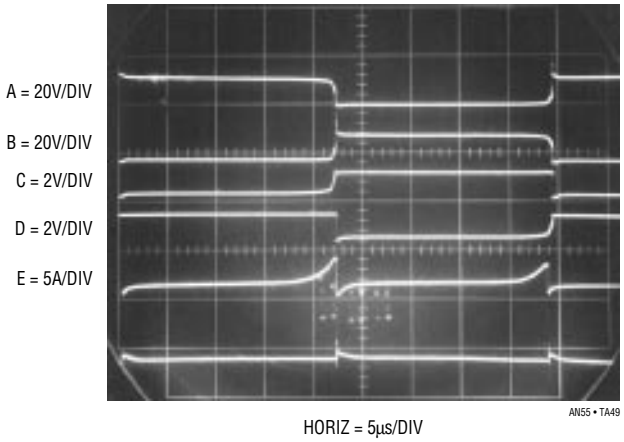

Figure I2. Waveforms for the Classic Royer Circuit

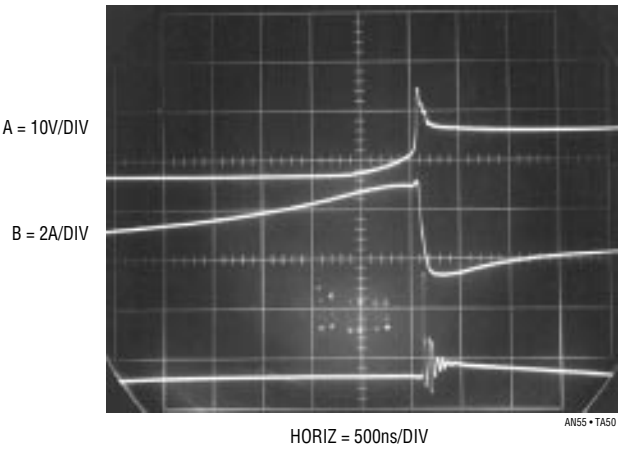

Figure I3. Detail of Transistor Switching. Turn-Off (Trace A) Occurs Just as Transformer Heads into Saturation (Trace B)

APPENDIX J

A LOT OF CUT-OFF EARS AND NO VAN GOGHS

Some Not-So-Great Ideas

The hunt for a practical CCFL power supply covered (and is still covering) a lot of territory. The wide range of conflicting requirements combined with ill-defined lamp characteristics produces plenty of unpleasant surprises. This section presents a selection of ideas that turned into disappointing breadboards. Backlight circuits are one of the deadliest places for theoretically interesting circuits the author has ever encountered.

Not-So-Great Backlight Circuits

Figure J1 seeks to boost efficiency by eliminating the LT1172's saturation loss. Comparator C1 controls a free running loop around the Royer by on-off modulation of transistor base drive. The circuit delivers bursts of high voltage sine drive to the lamp to maintain the feedback node. The scheme worked, but had poor line rejection due to the varying waveform vs supply seen by the RC averaging pair. Also, the "burst" modulation forces the loop to

constantly restart the lamp at the burst rate, wasting energy. Finally, lamp power is delivered by a high crest factor waveform, causing inefficient current-to-light conversion in the lamp.

Figure J2 attempts to deal with some of these issues. It converts the previous circuit to an amplifier controlled current mode regulator. Also, the Royer base drive is controlled by a clocked, high frequency pulse width modulator. This arrangement provides a more regular waveform to the averaging RC, improving line rejection. Unfortunately, the improvement was not adequate. 1% line rejection is required to avoid annoying flicker when the line moves abruptly, such as when a charger is activated. Another difficulty is that, although reduced by the higher frequency PWM, crest factor is still non-optimal. Finally, the lamp is still forced to restart at each PWM cycle, wasting power.

Figure J3 adds a "keep alive" function to prevent the Royer from turning off. This aspect worked well. When the PWM goes low the Royer is kept running, maintaining low level lamp conduction. This eliminates the continuous lamp restarting, saving power. The "supply correction" block feeds a portion of the supply into the RC averager, improving line rejection to acceptable levels.

This circuit, after considerable fiddling, achieved almost 94% efficiency but produced less output light than a "less efficient" version of text Figure 6! The villain is lamp waveform crest factor. The keep alive circuit helps, but the lamp still cannot handle even moderate crest factors.

Figure J4 is a very different approach. This circuit is a driven square wave converter. The resonating capacitor is eliminated. The base drive generator shapes the edges, minimizing harmonics for low noise operation. This circuit works well, but relatively low operating frequencies are required to get good efficiency. This is so because the sloped drive must be a small percentage of the fundamental to maintain low losses. This mandates relatively large magnetics—a crucial disadvantage. Also, square waves

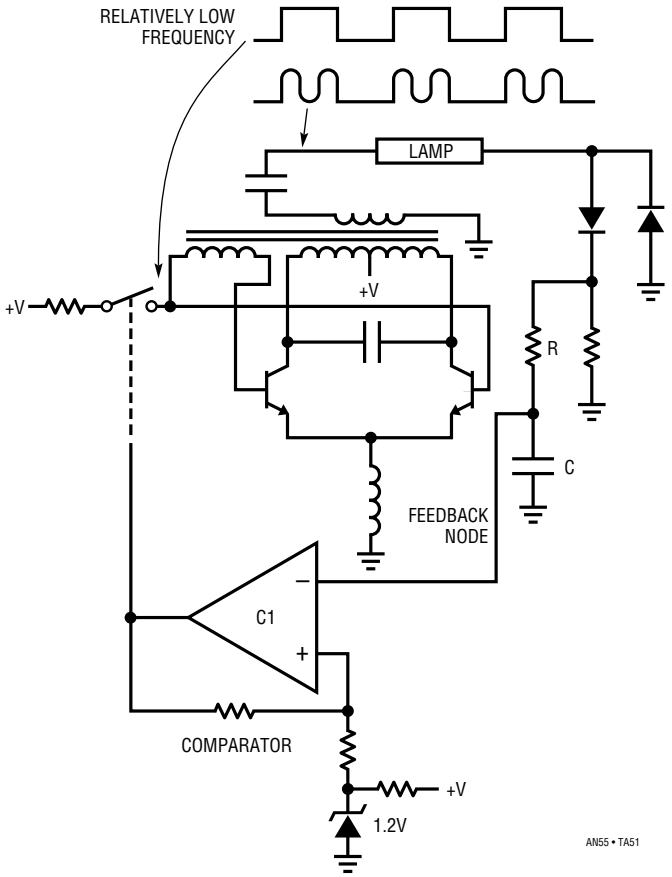

Figure J1. A First Attempt at Improving the Basic Circuit. Irregular Royer Drive Promotes Losses and Poor Regulation

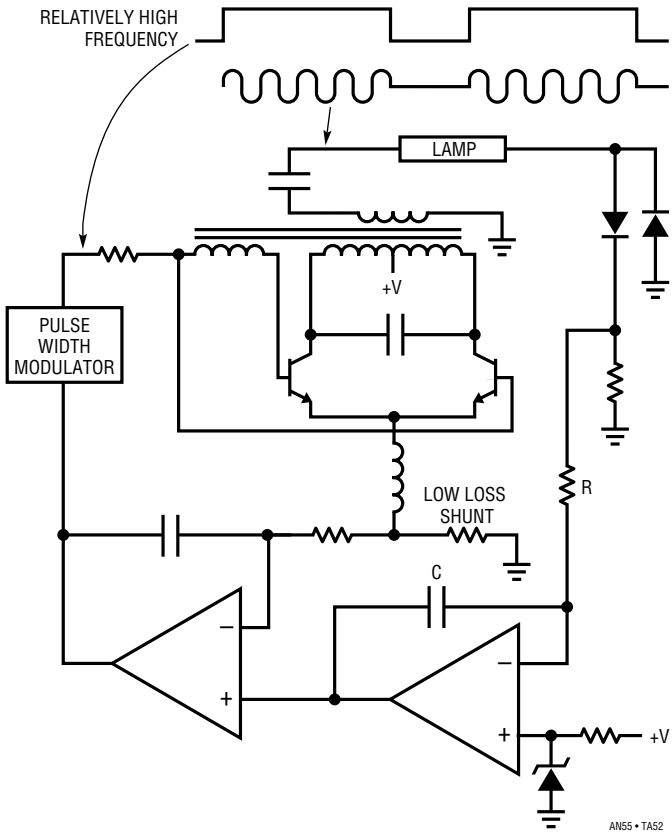

Figure J2. A more Sophisticated Failure Still has Losses and Poor Line Regulation

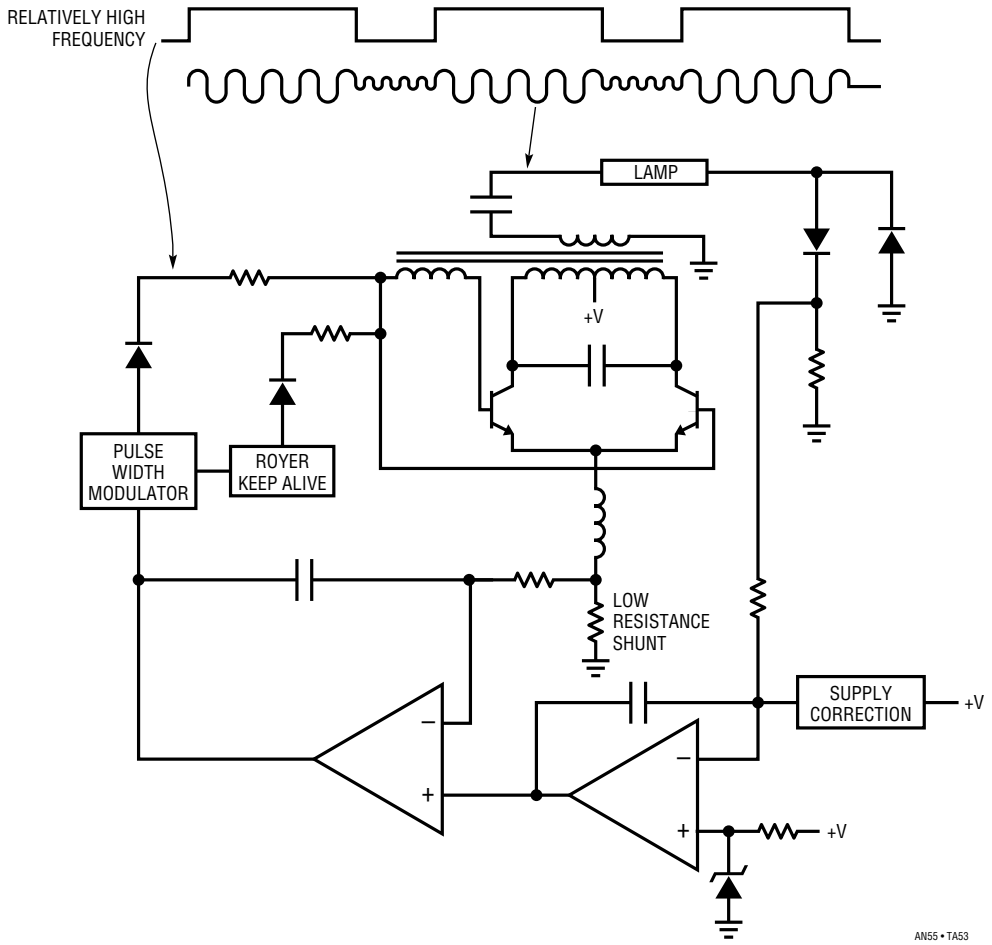

Figure J3. "Keep Alive" Circuit Eliminates Turn-On Losses and has 94% Efficiency. Light Emission is Lower than "Less Efficient" Circuits

have different crest factor and rise time than sines, forcing inefficient lamp transduction.

Not-So-Great Primary Side Sensing Ideas

Text Figures 28 and 29 use primary side current sensing to control lamp intensity. This permits the lamp to fully float, extending its dynamic operating range. A number of primary side sensing approaches were tried before the "top side sense" won the contest.

J5's ground referred current sensing is the most obvious way to detect Royer current. It offers the advantage of simple signal conditioning—there is no common mode voltage. The assumption that essentially all Royer current derives from the LT1172 emitter pin path is true. Also true, however, is that the waveshape of this path's current varies widely with input voltage and lamp operating current. The RMS voltage across the shunt (e.g., the Royer

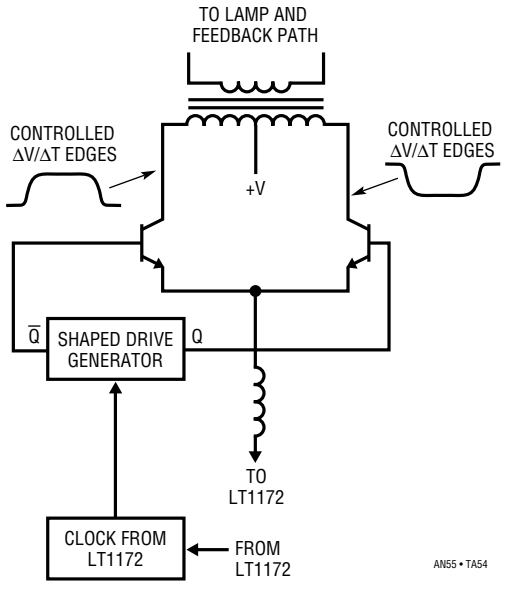

Figure J4. A Non-Resonant Approach. Slew Retarded Edges Minimize Harmonics, but Transformer Size Goes Up. Output Waveform is also Non-Optimal, Causing Lamp Losses

current) is unaffected by this, but the simple RC averager produces different outputs for the various waveforms. This causes this approach to have very poor line rejection, rendering it impractical. J6 senses inductor flux, which should correlate with Royer current. This approach promises attractive simplicity. It gives better line regulation but still has some trouble giving reliable feedback as waveshape changes. Also, in keeping with most flux sampling schemes, it regulates poorly under low current conditions.

Figure J7 senses flux in the transformer. This takes advantage of the transformer's more regular waveform. Line regulation is reasonably good because of this, but low current regulation is still poor. J8 samples Royer collector voltage capacitively, but the feedback signal does not accurately represent start-up, transient and low current conditions.

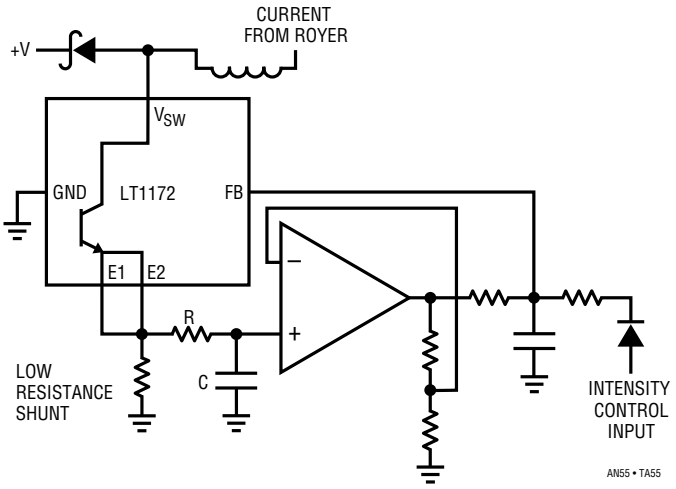

Figure J5. "Bottom Side" Current Sensing has Poor Line Regulation due to RC Averaging Characteristics

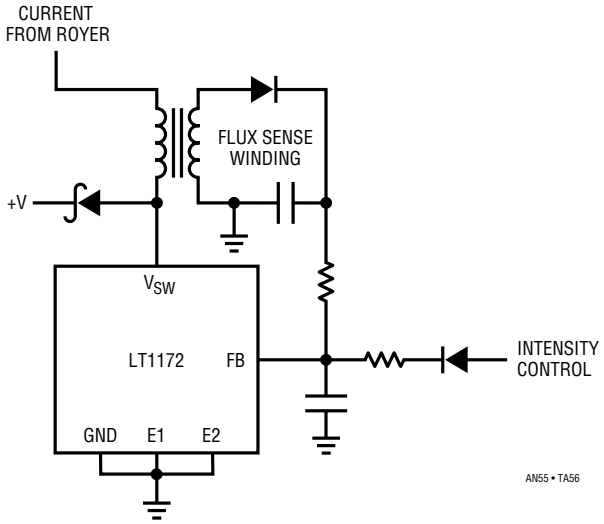

Figure J6. Flux Sensing has Irregular Outputs, Particularly at Low Currents

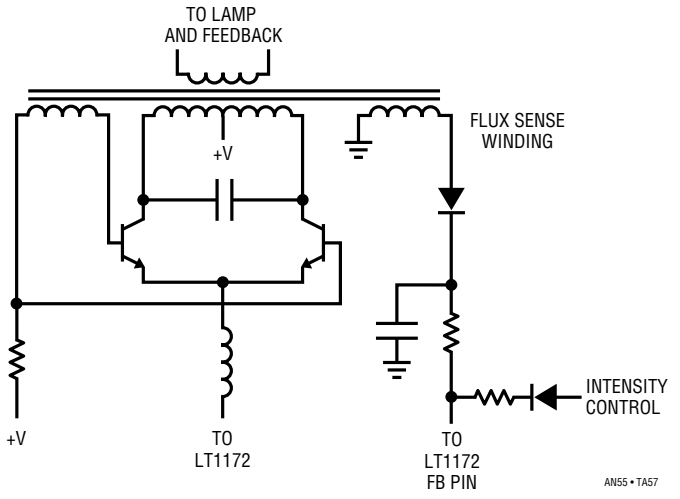

Figure J7. Transformer Flux Sensing Gives More Regular Feedback, but Not at Low Currents

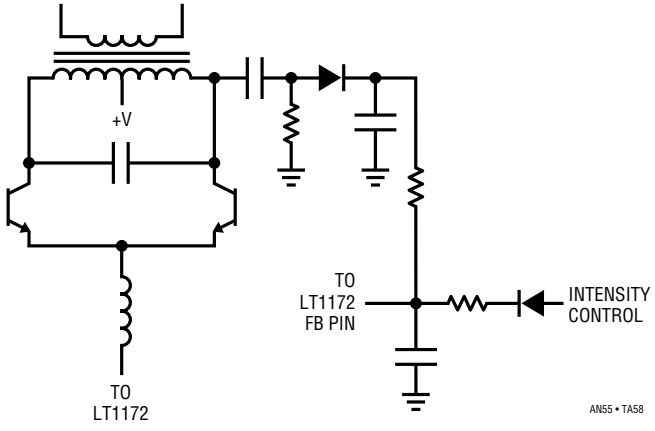

Figure J8. AC Coupled Drive Waveform Feedback is Not Reliable at Low Currents

APPENDIX K

PERSPECTIVES ON EFFICIENCY

The LCD displays currently available require two power sources, a backlight supply and a contrast supply. The display backlight is the single largest power consumer in a typical portable apparatus, accounting for almost 50% of battery drain with the display at maximum intensity. As such, every effort must be expended to maximize backlight efficiency.

The backlight presents a cascaded energy attenuator to the battery (Figure K1). Battery energy is lost in the electrical-to-electrical conversion to high voltage AC to drive the cold cathode fluorescent lamp (CCFL). This section of the energy attenuator is the most efficient; conversion efficiencies exceeding 90% are possible. The CCFL, although the most efficient electrical-to-light converter available today, has losses exceeding 80%. Additionally, the optical transmission efficiency of present displays is under 10% for monochrome, with color types much lower. Clearly, overall backlight efficiency improvements must come from lamp and display improvements.

Higher CCFL circuit efficiency does, however, directly translate into increased operating time. For comparison purposes text Figure 8's circuit was installed in a Toshiba Model 2200 running 5mA lamp current. The result was a 19 minute increase in operating time.

Relatively small reductions in backlight intensity can greatly extend battery life. A 20% reduction in screen intensity results in nearly 30 minutes additional running time. This assumes that efficiency remains reasonably flat as power is reduced. Figure K2 shows that the circuits presented do reasonably well in this regard, as opposed to other approaches.

The contrast supply, operating at greatly reduced power, is not a major source of loss.

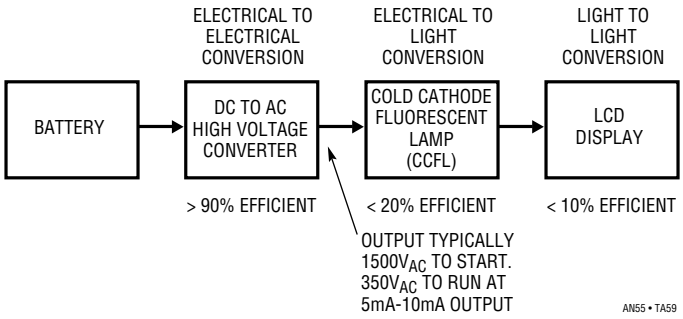

Figure K1. The Backlit LCD Display Presents a Cascaded Energy Attenuator to the Battery. DC to AC Conversion is Significantly more Efficient than Energy Conversions in Lamp and Display

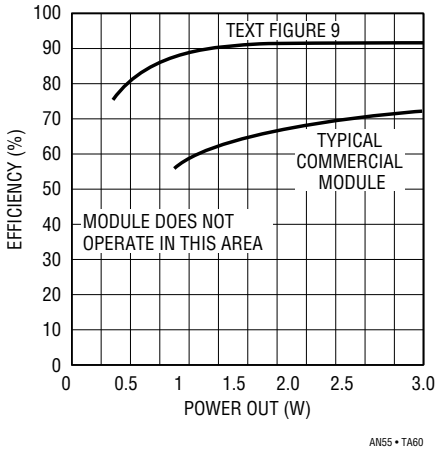

Figure K2. Efficiency Comparison Between Text Figure 9 and a Typical Modular Converter

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